June, 1980 ERC41005.24QR

# ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY

Quarterly Technical Report No. 11

For Period 01/01/80 through 03/31/80

Contract No. F49620-77-C-0087

Project No. 3384-2

Rockwell International/Electronics Research Center
Thousand Oaks, California 91360

Sponsored by:

Advanced Research Projects Agency (DOD)
ARPA Order No. 3384-2
Monitored by AFOSR under Contract No. F49620-77-C-0087

Prepared by:

F. H. Eisen
Principal Investigator

S. I. Long
Principal Investigator







Rockwell International

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

| REPORT DOCUMENTATION PAGE | READ INSTRUCTIONS BEFORE COMPLETING FORM |
|---|---|
| 1. REPORT NUMBER | 2. GOVT ACCESSION NO. ADA186884 — 3. RECIPIENT'S CATALOG NUMBER |
| 4. TITLE (and Subtitle) ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY | 5. TYPE OF REPORT & PERIOD COVERED Quarterly Technical Report 01/01/80 through 03/31/80 |
| | 6. PERFORMING ORG. REPORT NUMBER |
| 7. AUTHOR(s) R. Zucca, F. S. Lee, P. Asbeck, C. G. Kirkpatrick, C. P. Lee, Y. D. Shen, B. M. Welch, S. I. Long, F. H. Eisen | 8. CONTRACT OR GRANT NUMBER(s) F49620-77-C-0087 |
| 9. PERFORMING ORGANIZATION NAME AND ADDRESS ROCKWELL INTERNATIONAL/ELECTRONICS RESEARCH CENTER 1049 Camino dos Rios Thousand Oaks, CA 91360 | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS ARPA Order No. 3384-2 |
| 11. CONTROLLING OFFICE NAME AND ADDRESS Advanced Research Projects Agency (DOD) 1400 Wilson Boulevard Arlington, VA 22209 | 12. REPORT DATE May 1980 — 13. NUMBER OF PAGES 57 |
| 14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Air Force Office of Scientific Research Bolling Air Force Base Washington, DC 20332 | 15. SECURITY CLASS. (of this report) UNCLASSIFIED — 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE |

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

This research was sponsored by the Advanced Research Projects Agency (DOD) ARPA Order No. 3384

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Semi-insulating, Ion Implantation, ~~IC~~ Integrated Circuits, High Speed Logic, ~~GaAs~~ ~~FET~~ Gallium Arsenides

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the sixth quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The bulk of the work on this program is carried out at the Rockwell International Electronics Research Center (ERC). Significant assistance is provided by three subcontractors; Crystal Specialties Inc. in crystal growth, California Institute of Technology in ion implantation and related material technologies, and Cornell University in device modeling.

With MSI circuit complexity well demonstrated, the circuit development work in this quarter was focused on the testing of MSI/LSI circuits (250-500 gates),

over

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

and on the design of an LSI circuit (1000 gates). The preliminary data from the MSI/LSI circuits (from mask set AR4) are promising. Although the 5 x 5 bit parallel multiplier (260 gates) did not operate completely and did not function at its predicted speed, the test data indicate that it can meet the design expectations when a mask error (a missing connection on 16 gates) is corrected. The 2 x 32 stage shift register (550 gates) has functioned up to 33 stages involving approximately 300 gates. Further testing is scheduled. An 8 x 8 bit parallel multiplier (1008 gates) has been designed, layed out, and the mask set containing this circuit is being fabricated.

In the material supply area, while Bridgman grown Crystals Specialties material is widely used, the experiments with LEC grown material continue with good results in terms of doping profile uniformity across a wafer. Wafer fabrication on this material was started, on an experimental basis.

Studies on long term annealing of implanted layers, recoil implantation effects, crystal orientation effects on S implants in FET devices, and Si implantations are discussed in this report. A study of non-alloyed ohmic contacts carried out at CalTech is also reported. An improved technique for first to second layer metal interconnects based on anisotropic plasma etching of the vias and via filling with an intermediate metal layer is discussed. This technique will further improve the reliability of the interconnects. Promising radiation hardness data from ÷8 circuits are presented showing no appreciable performance changes after 5 x $10^7$ rad of total gamma dose.

TABLE OF CONTENTS

| | Page |
|---|---|
| FOREWORD | ii |
| TECHNICAL SUMMARY | iii |
| 1.0 INTRODUCTION | 1 |
| 2.0 SEMI-INSULATING MATERIAL | 3 |
| 2.1 Bridgman Material | 3 |
| 2.2 LEC Material | 7 |
| 2.3 Long Term Annealing Effects | 9 |
| 3.0 ION IMPLANTATION | 12 |
| 3.1 Recoil Studies | 12 |
| 3.2 Orientation Effects | 18 |
| 3.3 Si Implantation | 21 |
| 4.0 CIRCUIT FABRICATION | 25 |
| 4.1 Study of Non-Alloyed Ohmic Contacts to n-GaAs | 25 |
| 4.2 Improvements in Interconnect Fabrication | 27 |
| 5.0 CIRCUIT EVALUATION | 32 |
| 5.1 5 x 5 Bit Parallel Multiplier Evaluation | 32 |
| 5.2 2 x 32 Stage Shift Register Evaluation | 38 |
| 5.3 Yield of High Speed Circuits | 45 |
| 5.4 Radiation Hardness Assessment | 46 |
| 6.0 CIRCUIT DESIGN/8 x 8 MULTIPLIER ON MASK SET AR5 | 48 |
| 7.0 REFERENCES | 56 |

# FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Electronics Research Center as the prime contractor with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Forece Office of Scientific Research. The Rockwell program manager is Fred A. Blum. The principal investigators for each organization are:

| | |
|---|---|
| Electronics Research Center | F.H. Eisen, S.I. Long |
| California Institute of Technology | J.A. Mayer, M.A. Nicolet |
| Cornell University | L.F. Eastman |
| Crystal Specialties | W.P. Allred |

Numerous other researchers are involved in the work reported on. The principal contributors are:

| | |
|---|---|
| Electronics Research Center | P.M. Asbeck, R.C. Eden, A.Firstenberg, W.P. Fleming, J.A. Higgins, G. R. Kaelin, C.G. Kirkpatrick, C.P. Lee, F.S. Lee, M.J. Sheets, E.K. Shen, Y.D. Shen, E.R. Walton, B.M. Welch, R. Zucca |
| California Institute of Technology | B. Paine, M. Grimoldi |
| Cornell University | M. Shur |
| Crystal Specialties | J. Burns, H. Olsen |

## TECHNICAL SUMMARY

This report covers the sixth quarter, Phase II, of a program on ion implanted planar GaAs digital integrated circuit technology. The goal for Phase II of the program is to achieve the capability of fabricating GaAs ICs of LSI complexity. The fabrication approach, demonstrated in Phase I, is based on multiple localized implantations directly into the semi-insulating GaAs substrate to form active device areas insulated by the unimplanted regions of the substrate. The circuit concept, also demonstrated in Phase I, involves a combination of Schottky diodes and depletion mode Schottky barrier FETs, employed to form logic gates capable of high speed operation with very low power.

This program requires a research effort on all the multiple facets of process development. The research activities range from substrate growth and ion implantation technology to design fabrication, and evaluation of test circuits. These activities are carried out by the Electronics Research Center with the support of three subcontractors, California Institute of Technology, Cornell University, and Crystal Specialties, Inc.

During this quarter of this GaAs integrated circuit process development program, aging experiments on a capped, annealed sample were carried out at 230°C. No discernible change was observed in the Cr distribution beyond that which occurs during capping and post-implant annealing. A wafer fabrication lot of qualified LEC substrates was prepared (the LEC material was grown under a Rockwell IR&D program). The layout of the AR5 mask set, containing a 1000 gate LSI demonstration circuit, was completed. Evaluation of the 5 x 5 multiplier and 2 x 32 bit shift register circuits on AR5 was initiated. Preliminary results were very encouraging, with several chips showing nearly all of the 260 gates correctly functioning. Up to 300 gates were functional on a shift register chip. Yield and performance improvements are expected by modification of the Schottky metal mask to correct for minor design errors. These modifications will be incorporated prior to subsequent AR4 wafer lot processing. Preliminary radiation total dose assessment of 3 stage MSI divider circuits was conducted in

conjunction with RADC. No significant performance degradation was observed at doses as high as $5 \times 10^7$ rads, thus confirming the expected superior radiation hardness of GaAs digital ICs.

Materials and Fabrication

No discernible change in the Cr distribution was observed in SIMS measurements for a capped, annealed sample aged at 230°C for 500 hours.

SIMS bulk analysis study of ingots grown at Crystal Specialties with As from four different suppliers did not indicate any variation in the S content of the ingots.

LEC ingot R4 passed all qualification tests and looks promising for IC applications. A lot of R4 wafers are being prepared for fabrication. Other LEC ingots are being evaluated for IC use as well. The LEC ingots were grown under Rockwell IR&D funding.

SIMS results show good correlation with calculation performed by Cristel and Gibbons of Stanford for Si recoils produced by implanting Kr and Se thorugh $Si_3N_4$ for high doses ($2 \times 10^{14}$). No observable electrical effect of recoiled silicon has been measured for low dose through the cap implants ($2.5 \times 10^{12}$ $cm^{-2}$).

Preliminary studies of Si implants indicate that layers such as presently produced through S and Se implants can be fabricated reproducibly with Si for good activation and profile characteristics.

In the course of studies of electrical characteristics of GaAs MESFETs, it was noted that two identical FETs oriented in two difference directions on a (100) wafer may have different pinchoff voltages ($V_p$) and saturation currents ($I_{DSS}$). Low pinchoff voltage FETs were fabricated in four different directions with the n-type channel under the gate formed by 400 keV Se implantation at a typical dose of ~ 2x2 x $10^{12}$ ions/$cm^2$, with an additional S implant under the source and drain to form thicker $n^+$ regions. It was found that the FETs

oriented in the [011] direction always had lower $V_p$ and $I_{DSS}$, while the FETs oriented in the [01$\bar{1}$] direction had higher pinchoff voltages and saturation currents. The FETs parallel to the [010] and [001] directions had nearly identical characteristics, their values of $V_p$ and $I_{DSS}$ being between those of the [011] FETs.

Anisotropic etching of via windows is currently under development. This will result in via holes with nearly vertical sidewalls. The intermediate via hole metal is defined by depositing and lifting off a metal film of slightly less thickness than the second level dielectric. Sidewall coverage is no longer necessary for this filled via, hence the yield and reliability of second level metal to first level metal interconnects can be much higher when this approach is used. A denser second level metal interconnect layout is possible using this approach.

Preliminary evaluation has begun on the AR4 5 x 5 bit multiplier. It has been evaluated for logic functionality at low speeds using the MACSYM II automatic data acquisition system. All 1024 possible input combinations were exercised, and the ten output bit states were read and decoded for each test condition. Partial functionality of the circuit was observed with 773 correct products out of the 1024 total being obtained. This confirms that most of the 260 gates in the circuit were operating correctly. High speed testing was also attempted using the on-chip feedback mode. The circuit did exhibit full amplitude oscillations, however, the speed of the multiplier was much lower than normal.

During the course of the low speed logic functionality testing it was discovered that the AR4 5 x 5 multiplier contained a serious design error which left the pull-down active loads disconnected from $V_{SS}$ on 16 logic gates in the full adder array. It is certain that this error is responsible for the incomplete functionality and low speed observed. On the other hand, the data are very encouraging because they do not reveal any problem related to processing yield. The operating deficiencies are directly traceable to the design error.

The Schottky metal mask, the only mask level affected by the required design corrections, is now being replaced on mask AR4. The interconnect error has been repaired, and a new mask layer is presently being fabricated. This will allow the remaining lots of AR4 wafers, which were held before the Schottky metal layer process step, to provide test data on fully working, high speed multiplier circuits.†

The 2 x 32 bit shift register on mask set AR4 has also been evaluated on the first two wafer lots. This circuit contains 550 SDFL NOR gates. Partially functional shift registers with more than 33 contiguous registers functioning have been found. These devices operated in the serial loading mode and could recirculate data around one of the two 32 bit loops. In the 64 bit loop mode, data were shifted up to stage 34 before dropping out. This would indicate that over 300 contiguous gates are functioning properly. Minor design changes made on the AR4 Schottky metal mask should improve performance on subsequent wafer lots.

Three packaged divide-by 8 circuits were used for preliminary radiation hardness evaluation. These were irradiated at RADC to $Co^{60}$ total gamma doses of $10^6$, $10^7$ and $5 \times 10^7$ rad. The circuits were found to function properly with only small changes in the optimum bias voltages and corresponding currents. However, even these small changes could be attributed to tolerances in the test conditions. These excellent results confirm the expectation of superior radiation hardness for GaAs integrated circuits.

The design and layout of the 8 x 8 parallel multiplier circuit (mask set AR5), to be used as the final LSI demonstration vehicle for this program phase, was completed during the past quarter. Delivery of the masks is expected shortly. The multiplier array contains 48 full adders and 8 half adders for a total of 624 SDFL NOR gates. In addition, data input and output latches (16 of

---

†While this report was in press, measurements on AR4 wafers fabricated after the design error was corrected showed full operation (at good speed) of the 5 x 5 multiplier. The data will be provided in the next report.

each) were included to allow use of the device in a clocked data in/data out mode. The D flip-flop latches and additional buffer gates bring the total gate count up to 1008. The chip area is 2.8 mm x 2.35 mm including bonding pads.

# 1.0 INTRODUCTION

This report covers the sixth quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The program takes advantage of the superior electrical properties of GaAs in order to achieve high-speed low-power circuits. A fabrication technology based on ion implantation, using 1 m projection optical lithography, depending exclusively on dry etching processes, and making clever use of dielectrics to achieve a totally planar circuit structure has been implemented very successfully. Rapid progress in terms of circuit complexity was made since the start of the program, while meeting the original goals for circuit performance.

With MSI circuit complexity well demonstrated, the circuit development work in this quarter was focused on the testing of MSI/LSI circuits (250 - 500 gates), and on the design of an LSI circuit (1000 gates) which represents the final goal for this program phase in terms of circuit complexity. The preliminary data from the MSI/LSI circuits (from mask set AR4) are promising. Although the 5 x 5 bit parallel multiplier (260 gates) did not operate completely and did not function at its predicted speed, the test data indicate that it can meet the design expectations when a mask error (a missing connection on 16 gates) is corrected. The Schottky metal mask layer was remade for this correction, and wafers are in process. Despite the error, the circuit was able to yield 773 correct products of the 1024 possible combinations of two 5 bit factors.† The

†While this report was in press, measurements on wafers fabricated with the corrected mask showed full operation of the 5 x 5 multiplier, at high speed.

2 x 32 stage shift register (550 gate) has functioned up to 33 stages involving approximately 300 gates. Further testing is scheduled. An 8 x 8 bit parallel multiplier (1008 gates) with architecture and building blocks very similar to those of the 3 x 3 and 5 x 5 multipliers has been designed, layed out, and mask set AR5 containing this circuit is being fabricated.

In the material supply area, while Bridgman grown Crystals Specialties material is widely used, the experiments with LEC grown material continue with good results in terms of doping profile uniformity across a wafer. Wafer fabrication on this material was started, on an experimental basis.

Studies on long term annealing of implanted layers, recoil implantation effects, crystal orientation effects on S implants in FET devices, and Si implantations are discussed in this report. A study of non-alloyed ohmic contacts carried out at the California Institute of Technology is also reported. An improved technique for first to second layer metal interconnects based on anisotropic plasma etching of the vias and via filling with an intermediate metal layer is discussed. Promising radiation hardness data from 8 circuits are presented.

The bulk of the work on this program is carried out at the Rockwell International Electronics Research Center (ERC). Significant assistance is provided by three subcontractors; Crystal Specialties Inc. in crystal growth, California Institute of Technology in ion implantation and related material technologies, and Cornell University in device modeling.

# 2.0 SEMI-INSULATING MATERIAL

The supply of GaAs material is an issue of critical importance. The progress of various suppliers of ingots grown by the horizontal Bridgman method continues being monitored and material evaluated. Working with Crystal Specialties, analytical techniques have been applied to improving Bridgman growth. The purchase and operation of a new Metal Research crystal puller is expected to assist in improving the material supply. Preliminary results in LEC materials grown in the new system under an IR&D program are encouraging. The potential of both LEC and Bridgman materials for extension to large wafers are being considered.

## 2.1 Bridgman Material

An important consideration for uniformity and reproducibility in circuit characteristics is the uniformity of the semi-insulating ingots, both along ingot length and across a slice. It has been noted that samples from the front (seed end) portion of ingots typically show a lower qualification yield than corresponding tail samples. For use in the IC process, only ingots that pass the tests at both ends are accepted. Studies were carried out on the uniformity of several of these qualified ingots, using the depletion voltage $V_p$ (voltage required to deplete to a carrier density of $10^{16}$ $cm^{-3}$) resulting from a representative Se implant as the measure of ingot behavior. This is typically more sensitive than the profile depth. Figure 2.1-1 shows a plot of depletion voltage vs slice number in the ingot; uniform behavior is found over most of the ingot, with a slow decrease in $V_p$ towards the tail, as might be expected on the

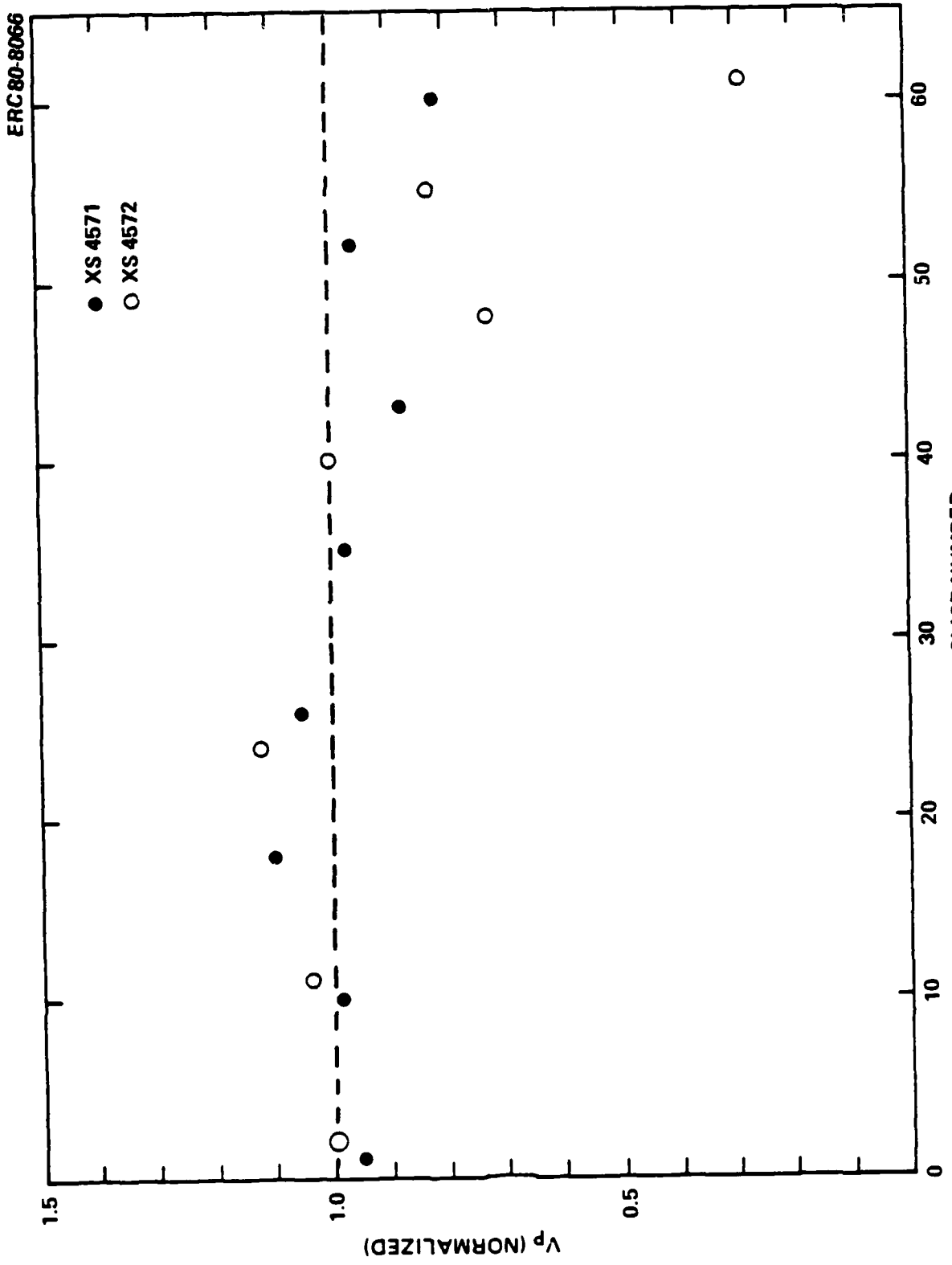



Fig. 2.1-1 Uniformity of Se implant results along ingot length of two Bridgman ingots.

basis of segregation effects. The uniformity of $V_p$ was also evaluated across an entire slice 2.3 inch wide by 1.6 inch high; these results are shown in Fig. 2.1-2. The standard deviation (obtained after omitting points within 3 mm of the edges) was 0.13 V. Within the area that would be occupied by the circuit of an IC wafer current size, the standard deviation was 0.05 V. The variations in pinchoff voltage around the mean also appear to reflect effects of segregation (the shape of the growing crystal does not coincide with the plane of the slice; the melt at the bottom of the boat freezes last). The results indicate a degree of uniformity within the limits required for fabrication of SDFL circuits. A possible avenue for further improvement of uniformity is to increase the melt size (from the current neighborhood of 1000 gm) inasmuch as this would spread the segregation effects over a larger volume of GaAs.

The most important factor in obtaining qualified Bridgman ingots appears to be the reduction of Si contamination in the melt due to the quartz growth boat and ampoule.[1,2] Direct chemical measurements of Si at the levels of interest ($10^{15}$ -$10^{16}$ $cm^{-3}$) has proven very difficult. However, bulk analysis by the SIMS technique (by Charles Evans & Associates) is a developing technique which appears to have the requisite sensitivity not only for Si but for most other impurities believed to be important in semi-insulating GaAs (with the exception of oxygen). Preliminary results indicate that the Si concentration tends to be lower towards the tail (last to freeze) section of Crystal Specialties ingots (for both Cr doped or undoped melts),[3] contrary to expectations from published distribution coefficients. Results suggest also that the sulphur content of the ingots may be high enough to be of significance in qualification ($2 - 5 \times 10^{15}$ $cm^{-2}$). A study of ingots grown with As (believed to be the

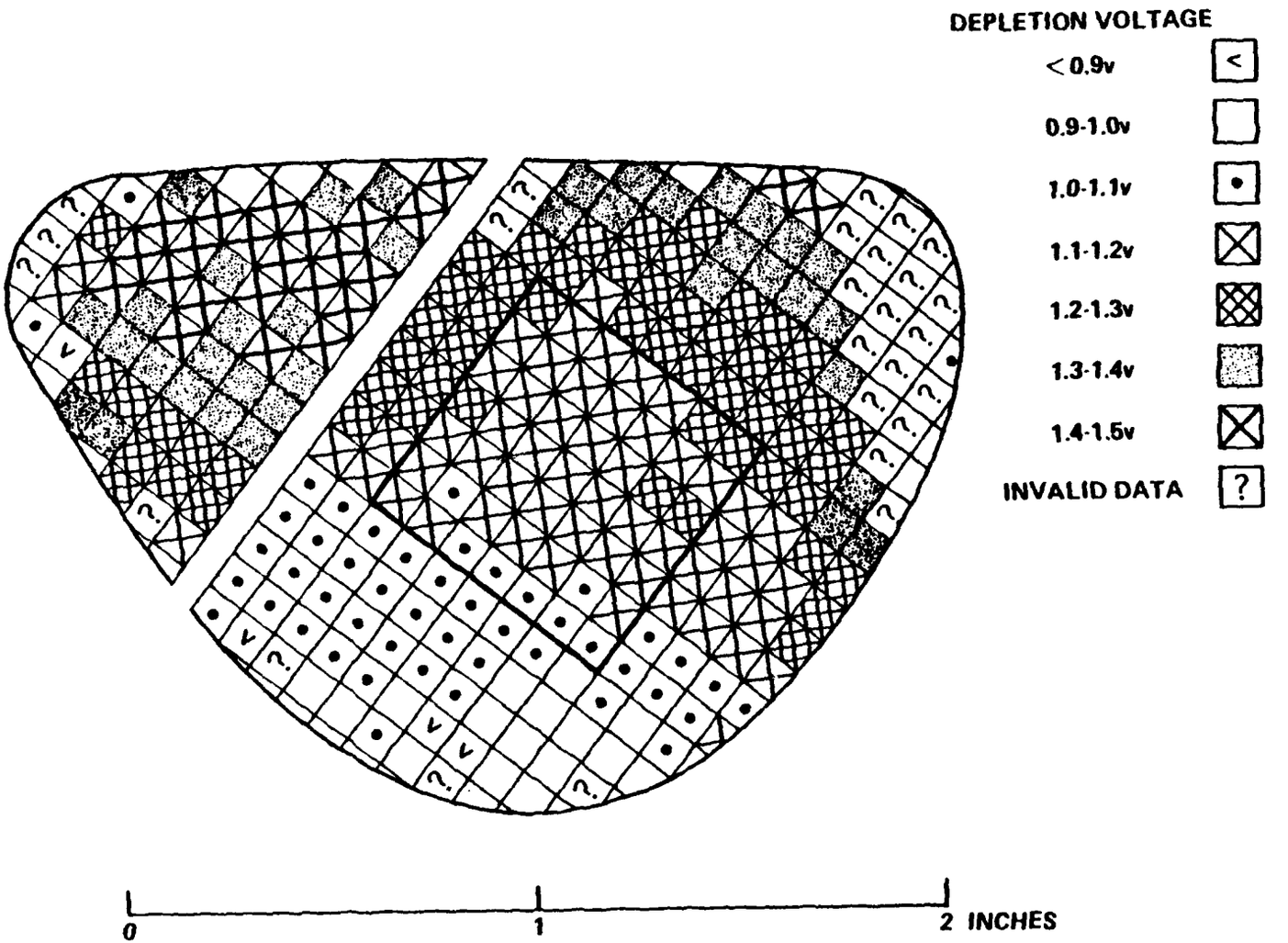



Fig. 2.1-2 Uniformity map of entire slice of Bridgman material indicating variations in depletion voltage. The square outline indicates the are a that would be occupied by an IC wafer.

primary source of S contamination) from 4 different suppliers, however, did not indicate any variations in the S content of the ingots. Investigations of this type appear to be worthwhile for understanding of sources of contamination and will be continued.

Additional research efforts have been carried out at Crystal Specialties to improve ingot yield. Ingots were grown with a moderate increase (x 2) in the amount of Cr added to the melt in order to decrease the percentage of ingots that fail to qualify at the seed end. Preliminary indications that this may be a successful technique have been obtained. Coating of quartz boats with a layer of $Si_3N_4$ also has been carried out. The Si contamination during growth in such a coated boat did not appear to be reduced; however, the use of both a coated boat and a coated ampoule remains to be attempted. Boat coatings may also be of benefit in reducing boat-wetting, a recurrent problem in the Bridgman growth, periodically causing twinning or polycrystalline growth.

## 2.2 LEC Material

Detailed qualification studies have been carried out on two ingots and are being applied to a third ingot of the liquid encapsulated Czochralski (LEC) material produced under an IR&D program.[3] These ingots passed the isolation qualification test. In Fig. 2.2-1, C-V profiles from one of these ingots illustrate the results of the Se profile tests. Profiles obtained from the other ingot (not shown in Fig. 2.2-1) resulted in slightly lower activation levels than those observed in the first ingot. Initial studies comparing (111) and (100) wafer characteristics as manifested through Se profiles have also begun.

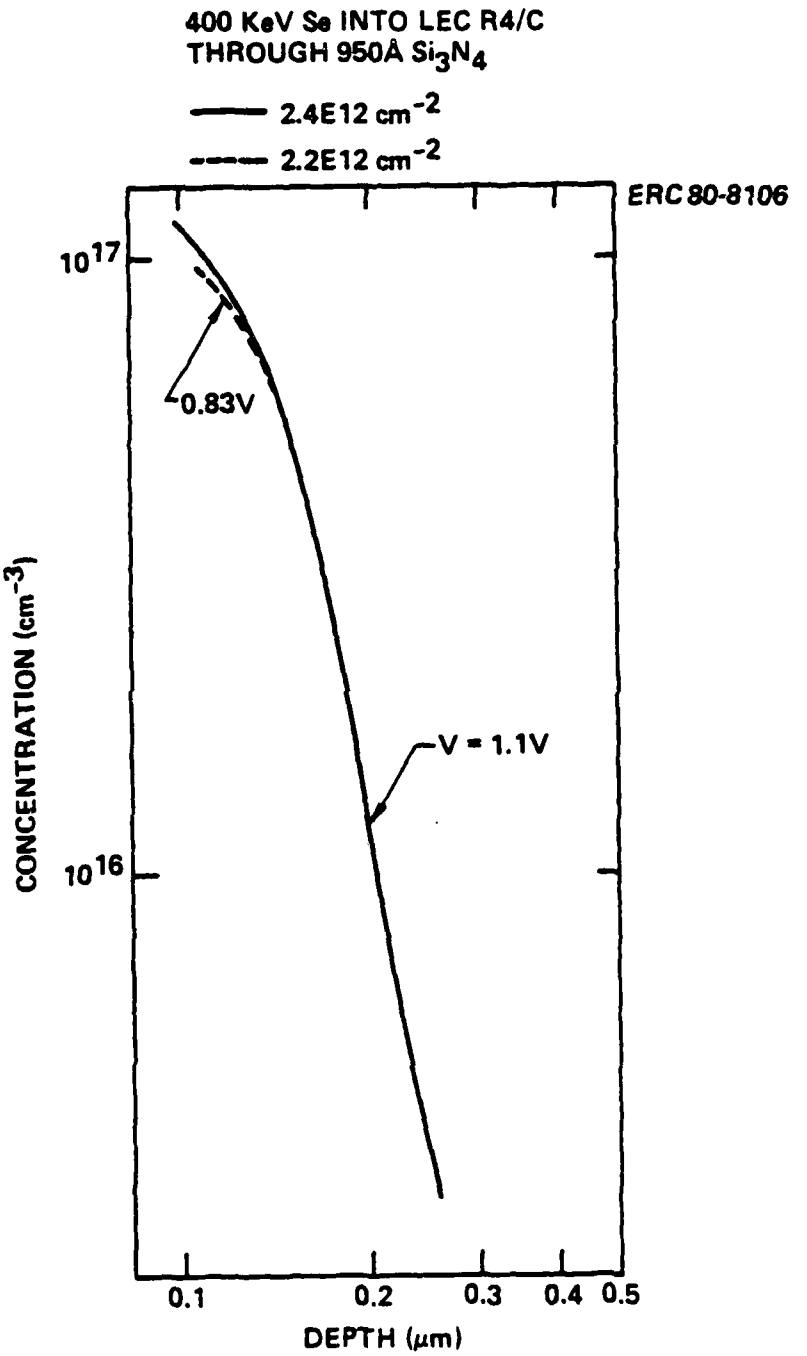



Fig. 2.2-1 Carrier concentration profiles obtained by implantation of Se at 400 keV into wafers from the LEC R4 ingot. The implantation was done through 950Å of $Si_3N_4$.

A lot of 4 wafers from one of the first two ingots is being prepared for fabrication. The third ingot, a large diameter one (3 in.), is also being studied for uniformity, with promising results. Large enough for 4 current size IC wafers per slice, the regions which would encompass the wafers showed reasonable deviations in $V_p$; as low as 45 mV per quadrant. Profiles from this ingot show good characteristics for the standard Se implants through $Si_3N_4$ as well.

## 2.3 Long Term Annealing Effects

A number of reported studies[4,5] have indicated that significant redistribution of Cr can occur at temperatures as low as 300°C under special circumstances (such as during alloying of GaAs with Au or after high dose implants). On the basis of these data one must be concerned about possible Cr redistribution near the surface of ion implanted FET channel layers during device aging, a redistribution which might lead to degradation of device characteristics.

In an effort to find whether prolonged, relatively low temperature anneals result in Cr redistribution in IC structures, several capped, Se implanted and annealed Cr doped samples were aged at 230°C for periods of 200 and 600 hours. SIMS studies were then performed at Charles Evans and Associates to determine whether these samples showed different Cr profiles from control samples processed similarly which did not undergo the "aging" heat treatment. No discernible change in the Cr distribution was observed. Figure 2.3-1 shows SIMS profiles for Cr for a control and an aged sample. Carrier densities profiles obtained by the C-V technique were also compared on the samples after removal of the encapsulant. Both profile shape and depletion voltage were

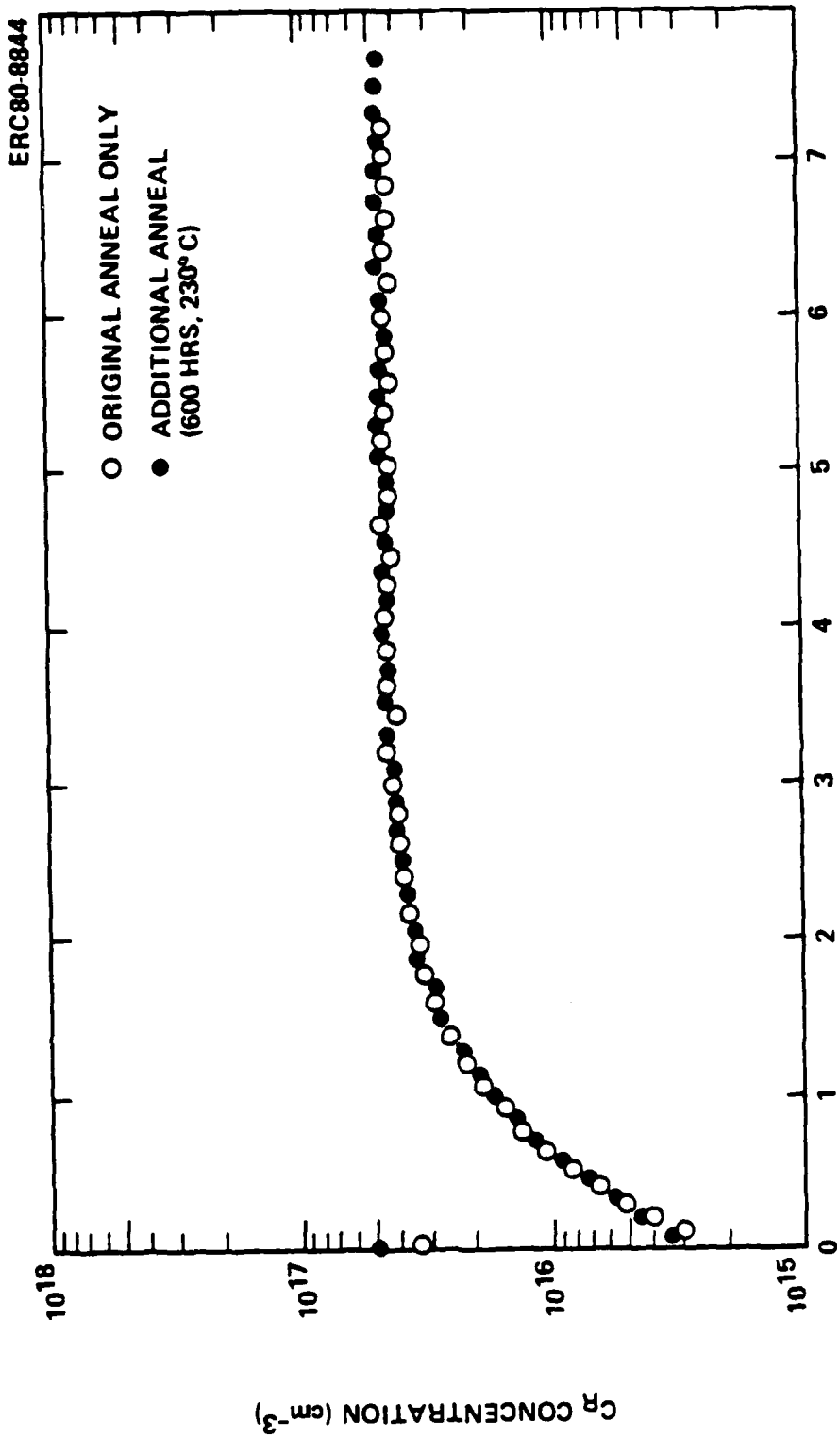



Fig. 2.3-1 SIMS profile of Cr concentration in an ion implanted sample which underwent additional anneal compared to a control sample.

identical between control and aged samples. From these data, it appears unlikely that Cr diffusion will contribute to circuit degradation.

# 3.0 ION IMPLANTATION

A vital part of the planar, high density GaAs IC process, ion implantation continues to be the subject of intensive activity. During this reporting period, studies were undertaken on a number of important topics relating to the successful application of implantation. Notable findings have been achieved in some cases; in other areas, the work is in the embryonic stage. Among the topics discussed in this section are recoil effects from implanting through the cap, crystal orientation effects, and Si ion implantation for $n^{++}$, $n^{-}$, and $n^{+}$ layers.

## 3.1 Recoil Studies

Although no direct evidence for concern about the possibility of recoils resulting from implantation through $Si_3N_4$ has been observed in this program, recoil is being investigated to determine potential effects on the type of implanted profiles utilized in the IC process. Relatively little work has been reported in the literature on this important subject. Studies have been undertaken in collaboration with J. Gibbons and L. Cristel of Stanford, where Boltzman transport calculations for through-nitride implants are being carried out. Experiments have begun at ERC to compare the results of theoretical predictions with fabricated layers.

In initial experiments, both electrical and SIMS data were analyzed for low fluence ($2.5 \times 10^{12}$ $cm^{-2}$) implants of Se and Kr both into bare substrates and through a 950A $Si_3N_4$ cap. In addition, N was implanted to determine

possible effects from nitrogen knock-ons in the material. These studies were directed toward determining whether the presence of tails in Se profiles might be due to the presence of Si atoms recoil-implanted into the near surface region of the GaAs substrate. The data from Gibbons and Cristel, shown in Fig. 3.1-1, indicated that at these low fluences, Si knock-ons may be present to a considerable depth into the sample. If electrically active, these Si ions would contribute to the carrier concentration profile ostensibly produced by Se ions, resulting in a tail. The preliminary studies showed no definite indication of the effect of recoil Si in the electrical data.

Carrier density near the surface of undoped (n type) GaAs substrates after capped and bare Kr implants (400 keV, 2.5 x $10^{12}$ $cm^{-2}$) and subsequent annealing was investigated. The calculated Si profile, if 100% electrically active, would induce a change of about 0.6 V between the voltages required to deplete Schottky barriers to a fixed depth (0.3 μm for convenience) on materials capped before and after the implant. An average shift (in the right direction) of only 0.3 V was observed, with rather larger error bars due to fluctuations in the background carrier density. Experiments of this type are being repeated to obtain more accurate results.

Si was observed near the surface in the SIMS measurements; however, it appeared to be likely due to residual Si from the nitride rather than a recoil effect. The sensitivity of the SIMS technique dictates the use of high fluence through nitride implants to produce a definite observable effect. Unfortunately, at these fluences, the electrical measurements become unwieldy due to poor dopant activation. However, in order to observe the effect and test the efficacy of the

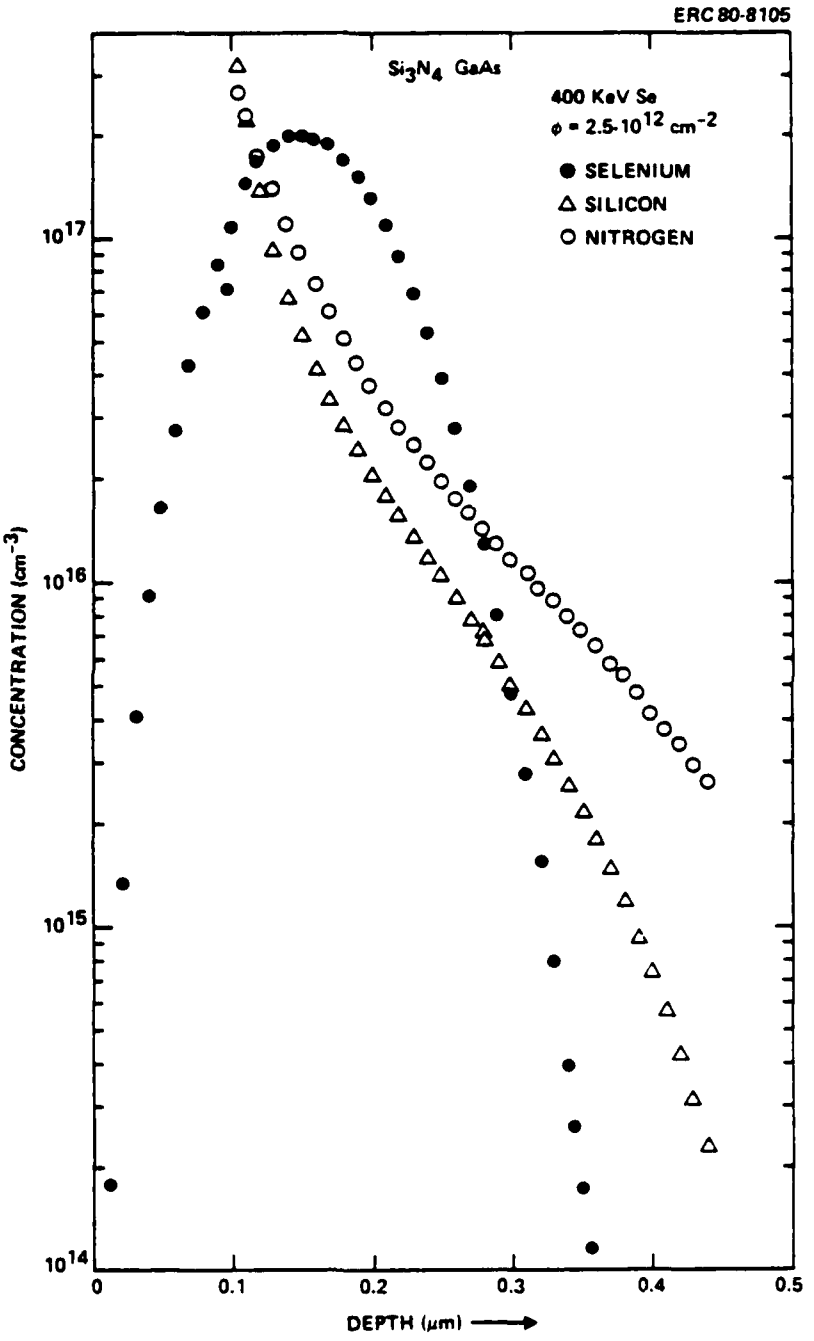



Fig. 3.1-1 Calculated profiles for atomic distribution of recoil Si and N for 400 keV Se implanted through 1000Å $Si_3N_4$ (from Gibbons and Cristel).

theoretical calculations, further SIMS studies were performed utilizing high fluence through the cap and bare Se and Kr implants so that the knock-on Si could be reliably profiled and compared to Stanford's calculations for these parameters.

For high dose experiments, undoped (100) GaAs samples from Crystal Specialties were encapsulated with 950A of silicon nitride. Control samples were also prepared without an encapsulation layer. Both capped and bare samples were implanted with either 400 keV Se or 400 keV Cr, to fluences of $2 \times 10^{14}$ or $2 \times 10^{15}$ ions/cm$^2$. After implantation, the silicon nitride was removed from the encapsulated samples and all samples received a gold evaporation. Atomic concentration profiles were measured by SIMS by Charles Evans and Associates.

The profiles resulting from these studies show close resemblance to the theoretical calculations. In Fig. 3.1-2, data for Se and Si profiles are shown for through cap implants. The data for $2 \times 10^{14}$ cm$^{-2}$ were shifted up by a factor of 10 for comparison purposes. The background concentration of Si has not been subtracted off from these profiles, limiting the range visible for low dose implants. New plots corrected for background Si will be soon available. The controls were free of surface Si accumulation except for recoils possibly resulting from contamination due to diffusion pump oil on the $2 \times 10^{15}$ cm$^{-2}$ Se implant. Plots for the calculations and experiments correlate quite well, except for the behavior close to the surface, and the absolute concentration.

The measured concentration profiles drop rapidly near the surface because the samples were coated with a layer of gold prior to profiling. The use of the gold successfully avoided spurious Si signals that appeared in earlier low dose work, probably due to dirt or incomplete $Si_3N_4$ removal.

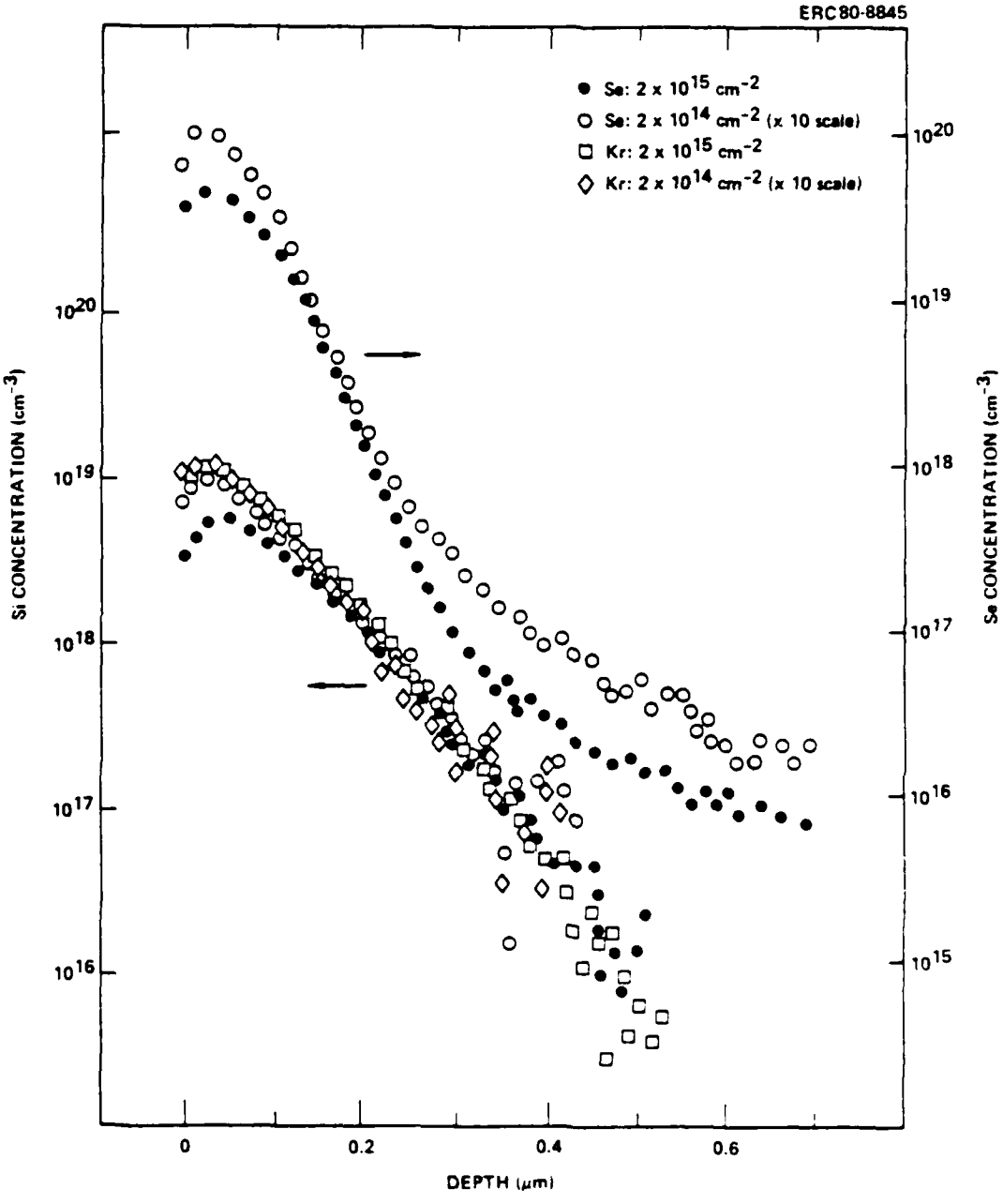



Fig. 3.1-2 SIMS profiles for high dose implants through a $Si_3N_4$ cap.

Features close to the surface are lost due to resolution limitations (of the order of 300A) either from crystal surface irregularities, ion mixing or cratering effects. Another technique problem is the uncertainty in the location of the cap-GaAs interface. The HF etchant used to remove the cap was found to attack the amorphous GaAs formed during implantation, so that it was hard to determine the etch endpoint. It is estimated that the samples may be overetched by < 250A.

The predicted and measured absolute concentrations differ by a factor of about 2 - 2.5. The Si calibration was done in reference to the As secondary ion count rate, with the proportionality factor determined by a Si implant profiled during the same session under similar sputtering conditions. The Se calibration was similarly obtained, by refering to the $2 \times 10^{15}$ $cm^{-2}$ bare Se implant. An a priori estimate for calibration accuracy is within a factor of 1.5 - 2. The principal calibration problem is sample charging, which can vary between samples and may affect secondary ion yields differently for different elements. Anomalous Se counts have also typically been found near sample surfaces, possibly due to chemisorbed oxygen. Thus, while the SIMS results tend to suggest that the number of recoiled Si atoms is slightly lower than calculated, the accuracy of the calculated concentrations is not disproven.

Evidence of recoiled N was also found in the SIMS measurements (by monitoring the $GaN^-$ molecular ion). The resulting count rate was, however, noisier, and there is not as consistent a picture of the N profile as there is for Si when comparing the results from all samples. The N calibration factor is uncertain at the moment; a reference implant will be measured.

In summary, recoil studies have been initiated to study the phenomenon and its potential effects, although these effects have not yet been manifest in results obtained through IC processes. Low fluence (in the range used for IC work) electrical studies did not indicate a contribution from recoiled components of the dielectric cap in carrier profiles. For high fluence SIMS studies revealed a correlation between observed and predicted Si recoil profiles. The indication thus far is that the recoiled Si is present but it is not electrically active in sufficient numbers to produce a discernible feature in the tail region.

## 3.2 Orientation Effects

In the course of studies of electrical characteristics of GaAs MESFETs, it was noted that two identical FETs oriented in two different directions on a (100) wafer may have different pinchoff voltages ($V_p$) and saturation currents ($I_{DSS}$). Low pinchoff voltage FETs were fabricated in four different directions (see Fig. 3.2-1) with the n-type channel under the gate formed by 400 keV Se implantation at a typical dose of $\sim 2.2 \times 10^{12}$ ions/cm$^2$, with an additional S implant under the source and drain to form thicker $n^+$ regions.

It was found that the FETs oriented in the [011] direction (FET A in Fig. 3.2-1) always had lower $V_p$ and $I_{DSS}$, while the FETs oriented in the [01$\bar{1}$] direction (FET B) had higher pinchoff voltages and saturation currents. The FETs parallel to the [010] and [001] directions had nearly identical characteristics, their values of $V_p$ and $I_{DSS}$ being between those of the [011] FETs.

SC79-5350

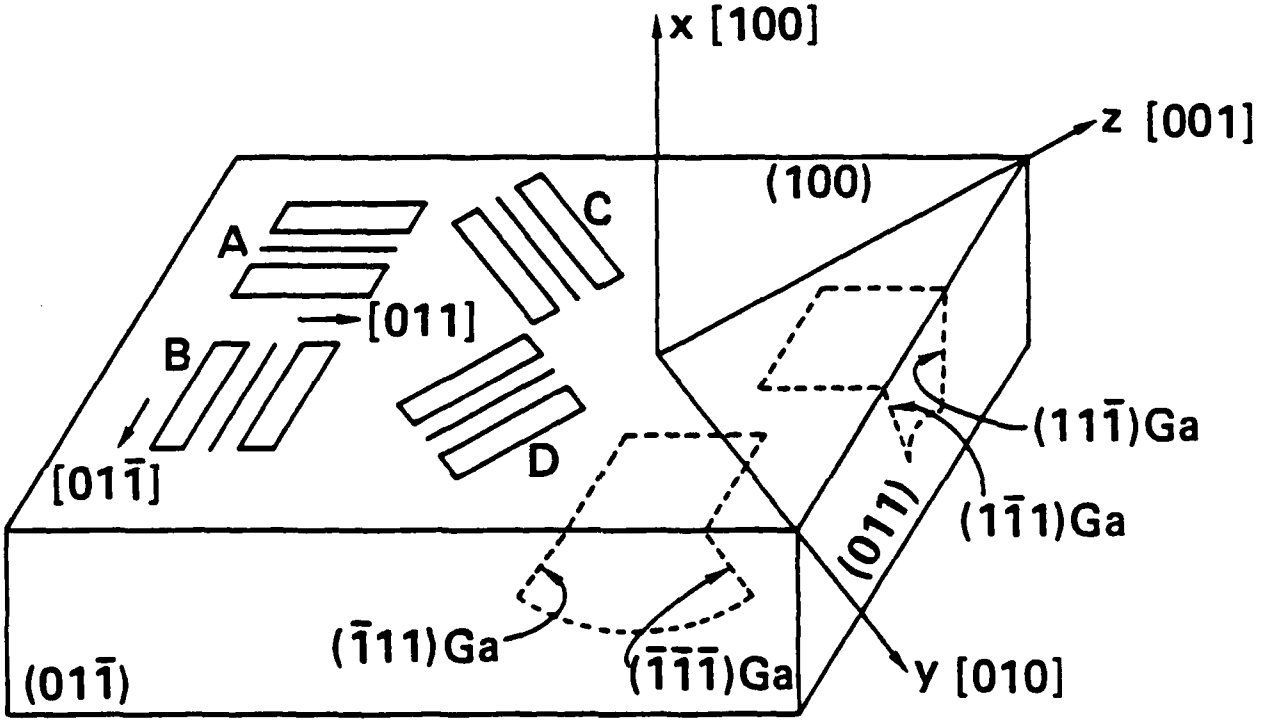



Fig. 3.2-1 Schematic drawing of the orientations of the FETs with respect to the GaAs substrate. A in [011] direction, B in [01$\bar{1}$] direction, C in [010] direction and D in [001] direction. The shapes of the etched grooves in two different [011] directions are shown by the dashed lines. The differences in the etched pattern enables us to identify the two different [011] directions.

It is well known that in GaAs, a zinc-blende crystal, the two [011] directions are not exactly equivalent while all the [100] directions are identical. While this property has been used to explain crystallographic properties, the effect on device performance has not been previously reported. Bulk GaAs, a cubic crystal, is electrically isotropic. At the interface between GaAs and the $Si_3N_4$ annealing cap, however, the anisotropy between the two [011] crystal directions may have an effect on the stresses due to the encapsulation layer. A differential in the stress due to direction may preferentially enhance lateral diffusion for the [011] case of the dopant S, which is known to diffuse during anneal,[6] in one direction more than another. Diffusion into the channel would affect the pinchoff voltage and saturation current, causing them to increase. A supporting observation for the lateral diffusion hypothesis was the data indicating that the difference between FET characteristics in the [011] and [01$\bar{1}$] directions was large for short gates and becomes smaller for longer gates.

These observations indicate several directions for further work. The FETs, of course, can all be oriented in the same direction on a wafer for uniformity of pinchoff voltage. However, studies verifying lateral diffusion phenomena as the cause for the observations need to continue. There are several approaches which may be applied to determine this. Among them, is examination of the difference in stress in the cap for the two different directions. Preliminary studies indicate that a differential in the stress may be observable. Another avenue is to try to directly observe the lateral diffusion in the channel through a technique such as induced current with a scanning electron

microscope. A third related subject for study is the examination of (111) material to determine if it shows similar effects and whether advantages may lie with the use of this particular orientation.

## 3.3 Si Implantation

The investigation of Si implantation for heavily doped contacts and as a possible replacement for both S and Se has continued. Si may offer several attractive features which make it a preferable alternative. Room temperature implantation of Si may activate better and be more reproducible for both channel and contact applications. A more controllable profile may be achieved with less diffusion with Si. In addition, the possibility of using only one implanted species throughout the process is a desirable feature from the point of view of manufacturing.

In addition to the heavy doping studies conducted previously at the California Institute of Technology,[2] work has been initiated at ERC to begin determination of the feasibility of replacing Se or S with Si throughout the process. Experiments have been done to simulate the type of profile developed with Se and S using Si, with positive results. In addition, test samples with various isotopes of Si and mass spectra studies have been performed to assure the purity of the Si beam in the 400 keV Extrion implantation system.

For fabrication of channel-type layers, Se and Si implants were carried out (in materials which were known to exhibit different degrees of "tailing" on the basis of previous Se implants) for a range of fluences and several energies. The results of these studies have been encouraging. Despite the lighter mass of

Si and therefore larger predicted straggle, the profiles are comparable to those from Se implants, exhibiting approximately the same shape and doping efficiency, as well as a high degree of the activation. An example of the profiles from these studies is shown in Fig. 3.3-1, in which Se and Si profiles are shown for the same substrate, cap, and anneal parameters. Profiles examined for both Si and Se showed approximately the same or less tailing for Si in ingots characteristically producing variations in profile depth.

These preliminary results indicate that Si implants for the channel are as suitable as Se for this application. Further experiments adjusting the dose and energy parameters to optimize the active layer are desirable. Studies regarding the reproducibility and uniformity of the Si implants are yet to be initiated, and the possible advantages to Si in these areas discerned.

Research has also involved the application of Si implantation to the diode and contact layers traditionally formed by S implantation. Here, the reprodubility of Si may be a key advantage to its use. Typical of the results of these initial studies are the curves of Fig. 3.3-2, in which doping profiles of deep Si implants through 950A of $Si_3N_4$ are shown. The data track well for increases in fluences and energy, and give indications of good reproducibility, and good activation. In addition to the experiments which serve to optimize the implant parameters to the application in the IC process, studies are under way to investigate the possible improvements and characteristics of this type of implant. Although room temperature implantation of Si appears to be entirely viable, hot (200°C) implants as well as room temperature implants of Si are being investigated for this medium fluence range.

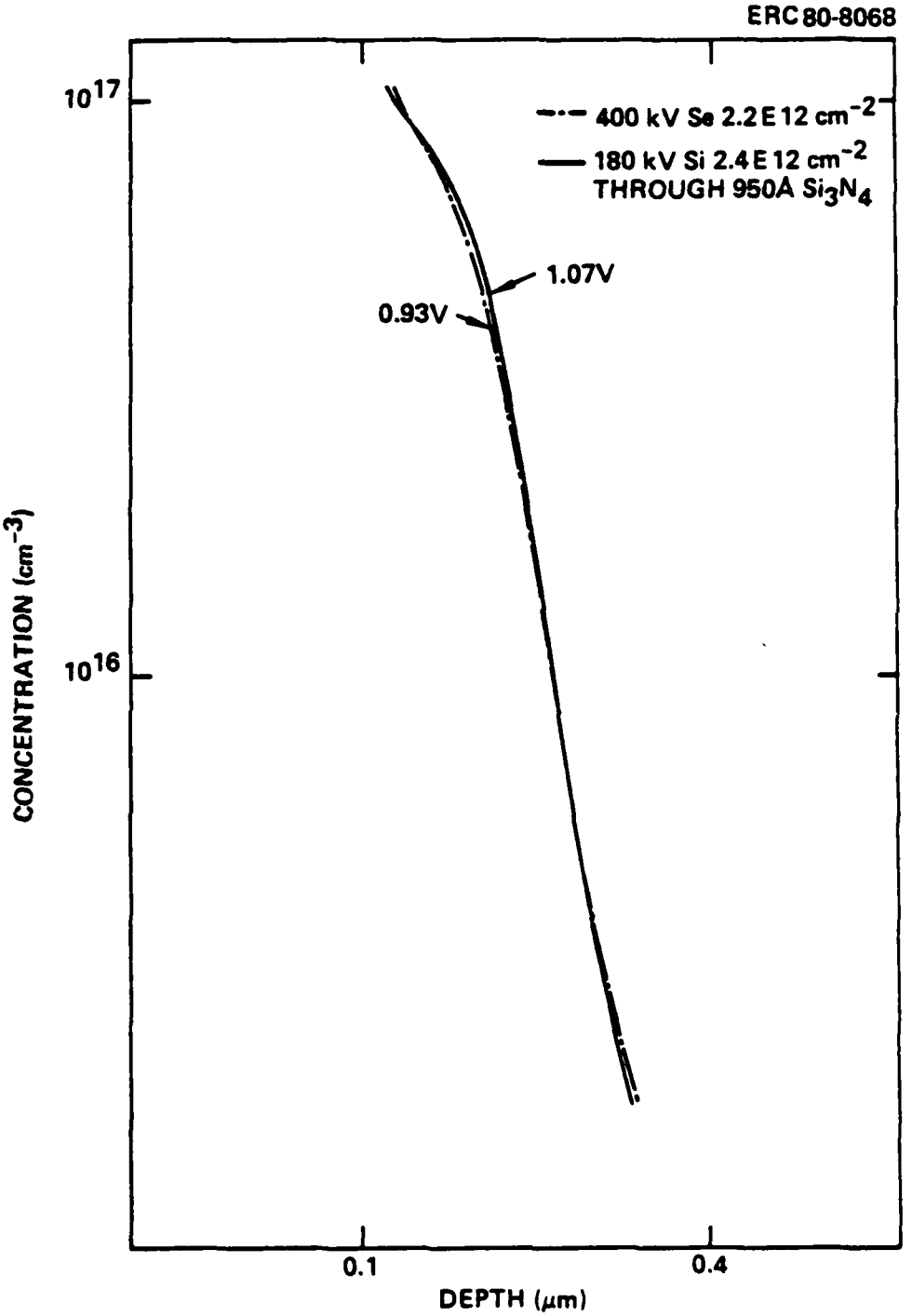



Fig. 3.3-1 CV profiles for Si and Se implants through 950Å $Si_3N_4$, annealed at 850°C for 30 minutes.

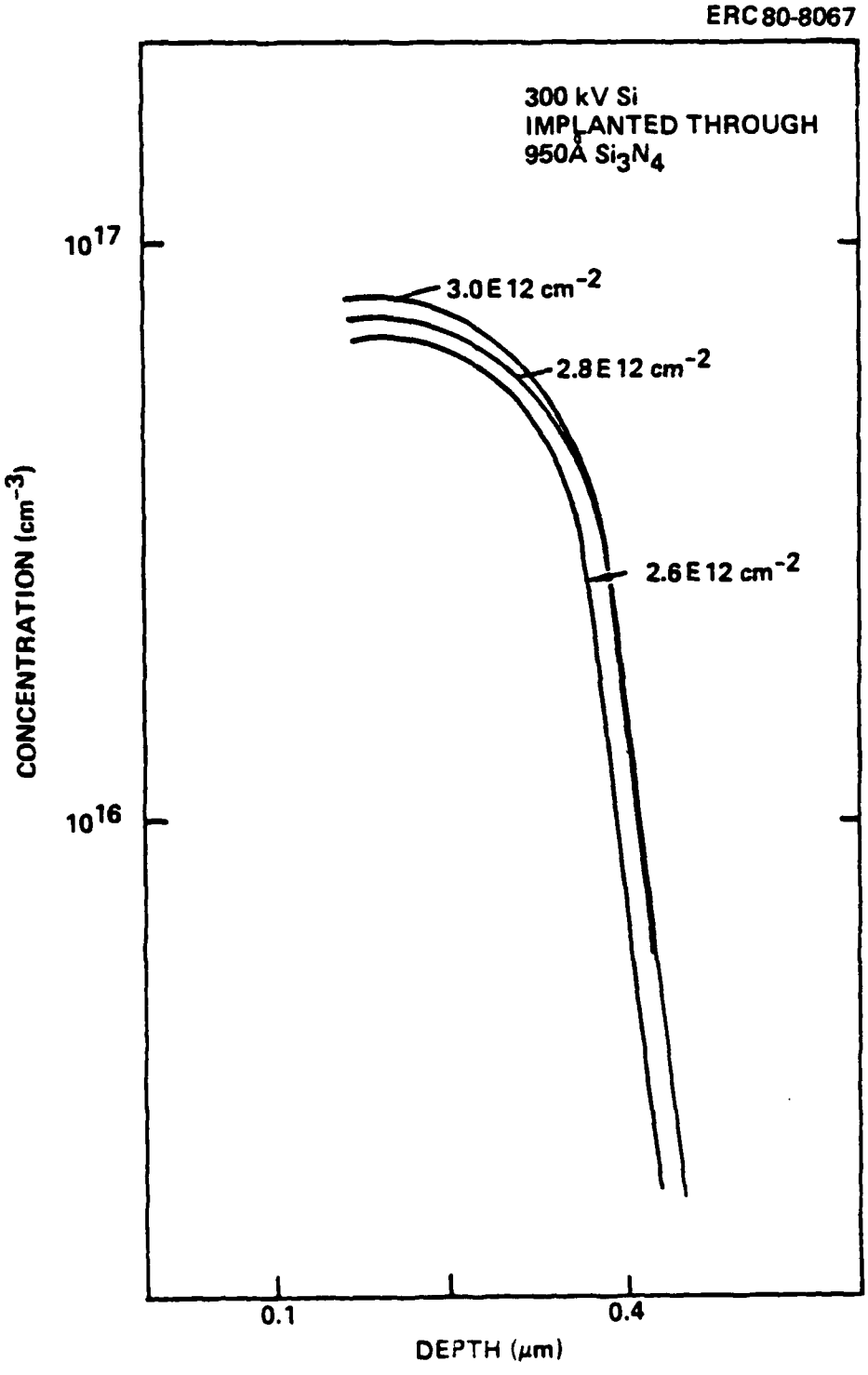



Fig. 3.3-2 CV profiles for 300 kV Si implants through 950Å $Si_3N_4$ annealed at 850°C for 30 minutes.

# 4.0 CIRCUIT FABRICATION

Fabrication of IC wafers has continued. At the same time tasks which are expected to lead to improvements in the process are being undertaken. Section 4.1 contains the results of a study of non-alloyed ohmic contacts carried out at Cal Tech. Although this work will not find an immediate application, this is an area of research worth exploring. A new approach to the fabrication of vias for interconnects between first and second level metallizations is discussed in Section 4.2. This technique is expected to further improve the reliability of the interconnects.

## 4.1 Study of Non-Alloyed Ohmic Contacts to n-GaAs

The ohmic contacts to planar devices are of decisive significance in the quality and reliability of monolithic circuits. Traditionally, such contacts are made to n-GaAs by depositing various metals and a dopant for GaAs on the GaAs substrate and heating above the melting point of the eutectic temperature. Some GaAs is then dissolved and the dopant is incorporated in the epitaxial growth upon cooling, thereby forming a degenerately doped layer. Both Ag-In-Ge and Aug-Ge alloys have been successfully used. Detailed studies have been performed on the Au-Ge-Ni contact.[7,8]

The basic premise in these procedures is that Ge goes substitutionally into Ga sites and produces a highly doped region under the metallic layer. In this study the role of Ge has been replaced by Si attempting to take advantage of the enhanced solid solubility of Si. Also, the Au was replaced by Pd and the two

elements were deposited in two consecutive evaporations, without breaking vacuum. The Si film was deposited directly onto the *n*-GaAs, and the Pd film was deposited on top of the Si film. The Pd films is known to form $Pd_2Si$ at rather low annealing temperatures (~ 200°).[9] It is also known that Pd films deposited on a Ge substrate forms $Pd_2Ge$ at similar low temperatures. Therefore, Pd films should also react at low temperatures with GaAs. In fact, it has been demonstrated that a Pd-Ge bilayer does react with GaAs and forms ohmic contact.[10] In contrast to the eutectic-forming metallization systems, these compound-forming layers do not melt during thermal annealing, thus offering the possibility of lateral unformity of the contact.

The n-type layers used for these experiments were obtained by 300 keV Se implantations into semi-insulating <100> GaAs at room temperature. Two doses of $3 \times 10^{12}$ $cm^{-2}$ and $5 \times 10^{13}$ $cm^{-2}$, were used. After implantation, the samples were capped with reactively sputtered $Si_3N_4$ and anneald at 850°C for 30 min in an $H_2$ ambient. Three different Si-Pd bilayered films were deposited to vary the Si:Pd ratio because it is expected that the product of the reaction will depend on this ratio. The three bilayers used had a Si:Pd ratio of 0.3 (500A Si and 1225A Pd), 0.5 (500A Si and 735A Pd), and 0.8 (500A Si and 460A Pd).

Contact patterns were then generated conforming to the transmission line model technique for specific contact resistance measurement.[11] The contacts were formed by sintering at 450°C for 10 min in vacuum (~ $10^{-6}$ Torr).

The results of a first set of measurements of the specific contact resistance are summmarized in Table 4.1-1.

Table 4.1-1 Specific Contact Resistance ($\Omega cm^2$).

| Se Dose 300 keV, R.T. | Si:Pd Ratio 0.3 | 0.5 | 0.8 |
|---|---|---|---|
| $3 \times 10^{12}$ $cm^{-2}$ | $3.0 \times 10^{-3}$ | $12 \times 10^{-3}$ | unreliable data |
| $5 \times 10^{13}$ $cm^{-2}$ | $7.6 \times 10^{-3}$ | $12 \times 10^{-3}$ | unreliable data |

It is observed that the values are in the $10^{-3}$ $\Omega cm^2$ range, which is much higher than Au-Ge-based contacts ($10^{-5}$ to $10^{-6}$ $\Omega cm^2$). It is also apparent that the specific contact resistance decreases with increasing amounts of Pd. This is consistent with the hypothesis that $Pd_2Si$ forms first, requiring, at least, a Si:Pd ratio of 0.5. Significant in these findings is the fact that ohmic contact behavior can indeed be obtained by solid-phase reactions of Si/Pd bilayers with n-GaAs. It would be desirable to investigate the lateral uniformity of these reacted layers on a microscopic scale, and to find out how much the specific contact resistance can be reduced by varying the parameters of the system (i.e., Si:Pd ratio, thermal annealing cycle, annealing ambient).

## 4.2 Improvements in Interconnect Fabrication

Vias required for connecting the first level interconnects to the second level interconnects are opened by reactive ion etching (RIE). The first level metal (Au) serves as an automatic etch stop; it also provides good adherence to the second level metal since a small amount of Au is sputtered during the RIE process.

The reactive ion etching of plasma nitride can be tailored to produce isotropic or anisotropic etched profiles depending on the plasma etching paramaters used. Currently isotropic etching is used; the sidewall of the etched vias are sloped as shown in Fig. 4.2-1(a). In conventional processing, sloped holes are necessary since the current path between the second level metal and first level metal must pass over the sidewalls of the via. The yield and reliability of the interconnect depends on the integrity of the sidewall coverage. Planetary e-beam evaporation or magnetron sputtering is used to ensure good metal sidewall coverage. The disadvantage of using a 60° sidewall via slope is that a 1 μm x1 μm interconnect to the first level metal requires the top of a 5000A thick 2nd level dielectric to be 1.5 μm x 1.5 μm. Therefore the dimensions of via holes are actually larger than needed. With a 0.5 μm alignment tolerance, the second level metal has to be at least 2.5 μm wide to cover a 1 μm x1 μm via. Although this is a workable approach, it is rather detrimental to the circuit density required for LSI/VLSI.

Anisotropic etching of via windows is currently under development. Figure 4.2-1(b) shows an anisotropically etched via hole with nearly vertical dielectric sidewalls and negligible undercut. Intermediate via hole metal is defined by depositing a metal film of slightly less thickness than the second level dielectric, followed by a lift-off process. This process scheme results in a planar structure as shown in Fig. 4.2-2. Sidewall coverage is no longer necessary for a filled via, hence the yield and reliability of second level metal to first level metal interconnects can be much higher when this approach is used. Since the via does not have any undercut (anisotropic), and there is no

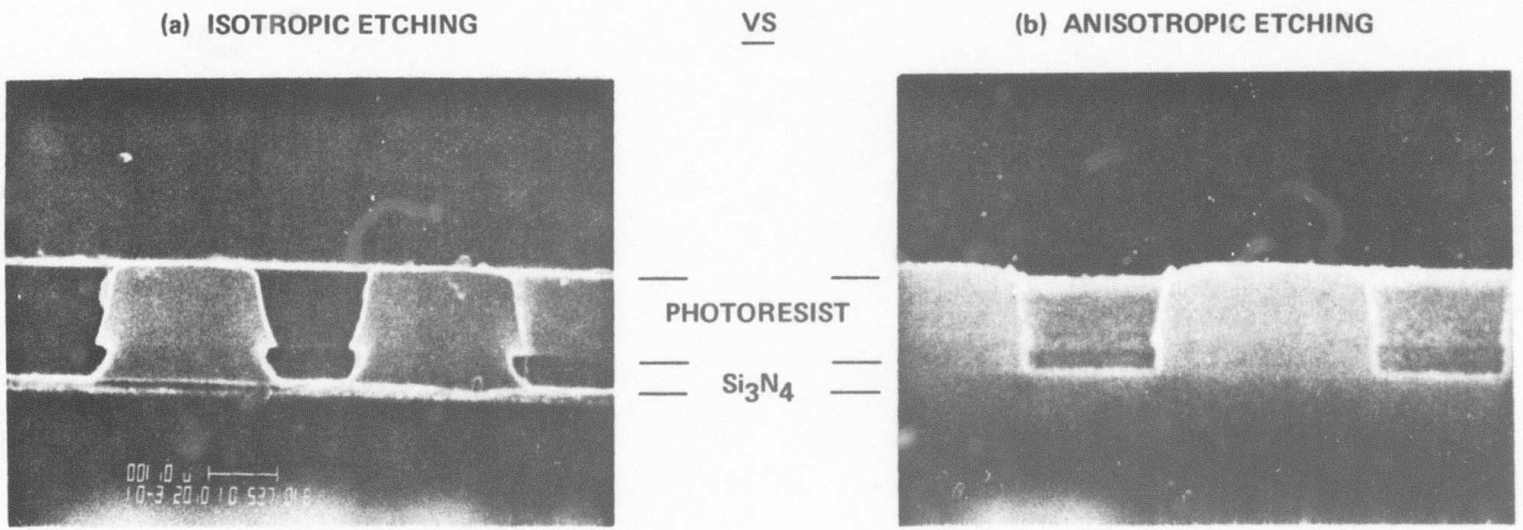



Fig. 4.2-1 Scanning electron micrograph of the reactive ion etched plasma nitride (5000Å thick) before the removal of the photoresist; (a) isotropic etching; (b) anisotropic etching.

ERC80-8114

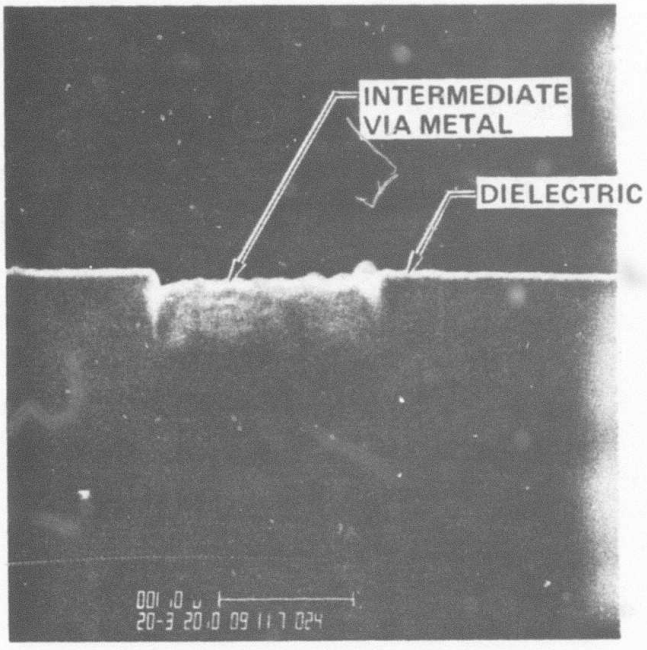



Fig. 4.2-2 Scanning electron micrograph of the cross section of an anisotropically etched and then filled via window.

step coverage, a denser second level interconnect is possible. This unique via approach is promising for ultra dense, high yield LSI/VLSI circut. Continued investigation and development of this structure will shortly lead to its incorporation into the standard planar process.

# 5.0 CIRCUIT EVALUATION

Evaluation of circuits on mask set AR4 has begun. These circuits are a 260 gate 5 x 5 bit parallel multiplier (discussed in Section 5.1) and a 550 gate 64-stage shift register and pseudo-random code generator (discussed in Section 5.2). Preliminary results are promising as they show that the process yield can meet the requirements of these high gate count circuits. However, mask errors have prevented the multiplier circuit from realizing all its potential in terms of speed. The Schottky metal mask has been replaced, and wafers now under process are expected to realize the full potential of this circuit. Some circuit yield information provided by the measurement of ÷8 circuits is discussed in Section 5.3. Preliminary data from radiation hardness experiments on ÷8 circuits indicating they can easily withstand total gamma doses of $5 \times 10^7$ rads are reported in Section. 5.4.

## 5.1 5 x 5 Bit Parallel Multiplier Evaluation

Evaluation of the 5 x 5 bit parallel multiplier on mask set AR4 has begun. A photomicrograph of a 5 x 5 multiplier chip is shown in Fig. 5.1-1. This circuit has a total gate count of 260. The operations required to multiply two 5-bit binary numbers ($B_4B_3B_2B_1B_0 \times A_4A_3A_2A_1A_0 = P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$) are illustrated in Fig. 5.1-2. The addition process in the multiplication is accomplished by properly combining full adders (FA) and half adders (HA) as shown in Fig. 5.1-2. Five half adders and fifteen full adders are used.

SC80-7680

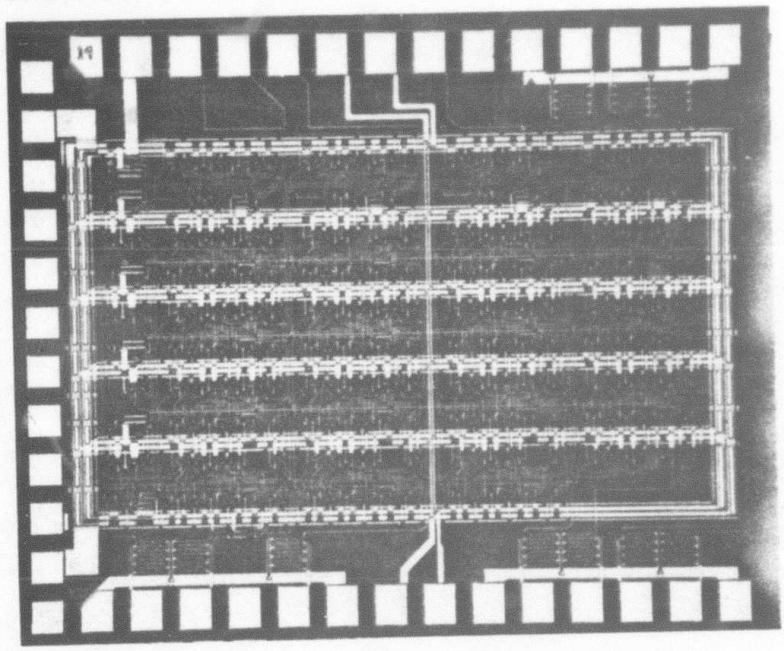


Fig. 5.1-1 SEM photograph of the 5 x 5 bit parallel multiplier on mask set AR4.

SC79-6265

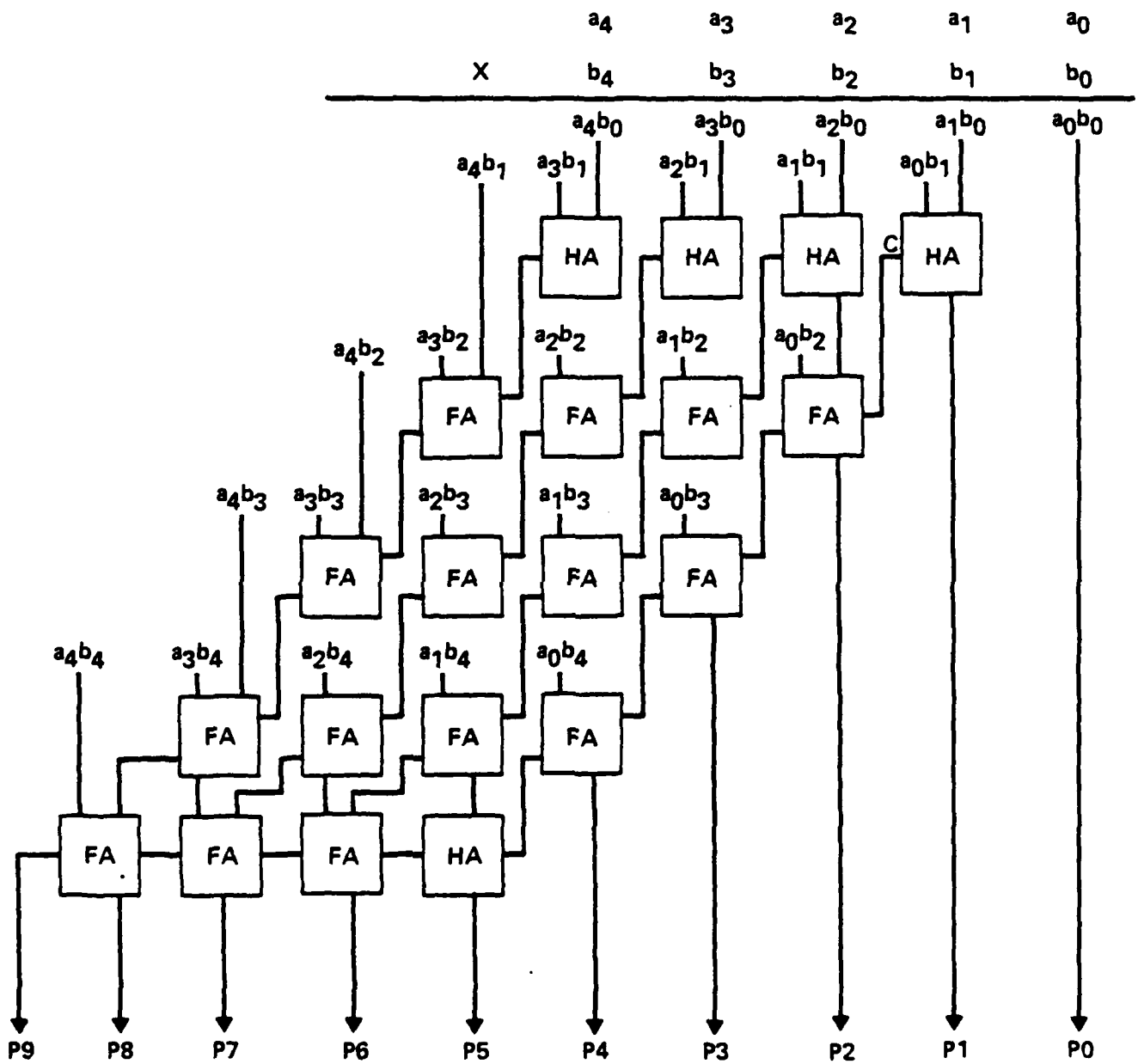



Fig. 5.1-2 Logic diagram of the 5 x 5 bit parallel multiplier on mask set AR4.

Two NOR control gates and a feedback path from $P_9$ (the most significant bit of the product) to $B_0$ (the least significant bit of multiplier) have again been added to provide a high speed feedback operating mode to assist in high speed evaluation as shown in Fig. 5.1-3. By presetting the multiplicand $B_4B_3B_2B_1B_0$ to 10000, the multiplicand $A_4A_3A_2A_1A_0$ to 11111, and setting the feedback enable control to "high", the multiplier will oscillate in the feedback mode. An oscillating frequency of $1/44\tau_d$ is expected. To ease the presetting of inputs A and B, an optional common input line (feedback mode preset) is connected to the $A_0$,$A_1$,$A_2$,$A_3$,$A_4$ and $B_4$ input NOR gates, so that all these inputs can be preset simultaneously through the common input line. With the feedback enable control gate set to "low", the data of $P_9$ will not be able to feed to $B_0$ through the feedback loop, so that the normal multiplier operation will be resumed.

The 5 x 5 bit multiplier has been evaluated for logic functionality at low speeds using the MACSYM II automatic data acquisition system discussed in Ref. 2. All 1024 possible input combinations were exercised and the ten output bit states were read as analog signals and decoded for each test condition. Partial functionality of the circuit was observed with 773 correct products out of the 1024 total being obtained. This confirms that most of the 260 gates in the circuit were operating correctly. Figure 5.1-4 shows the results obtained from setting the feedback preset input and toggling input $B_0$ with a pulse input "S". The product shown in the figure (A = 11111, B = 1000S) is performed with all 10 outputs responding properly. This verifies that the sum and carry outputs of all adders are being properly generated.

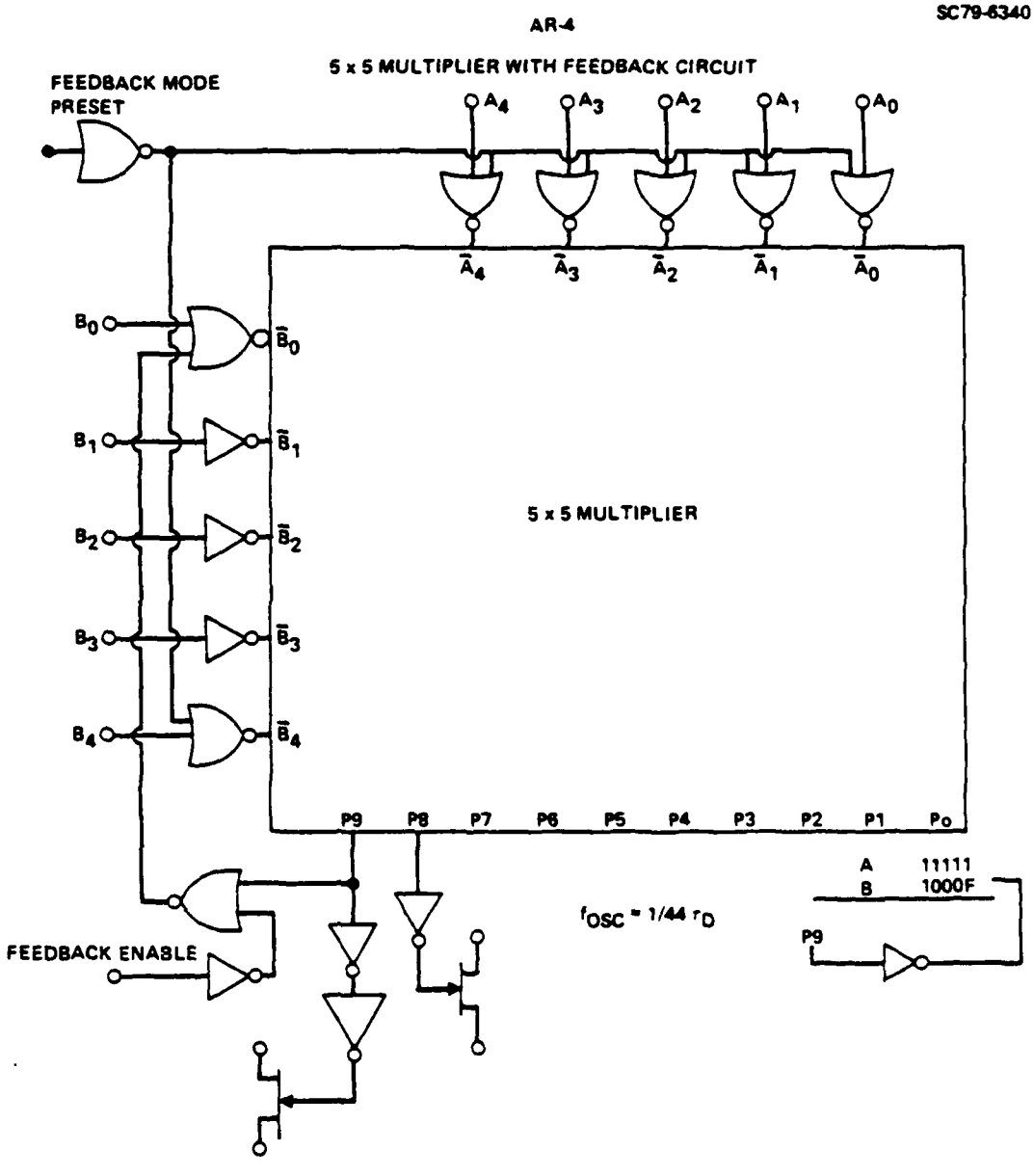
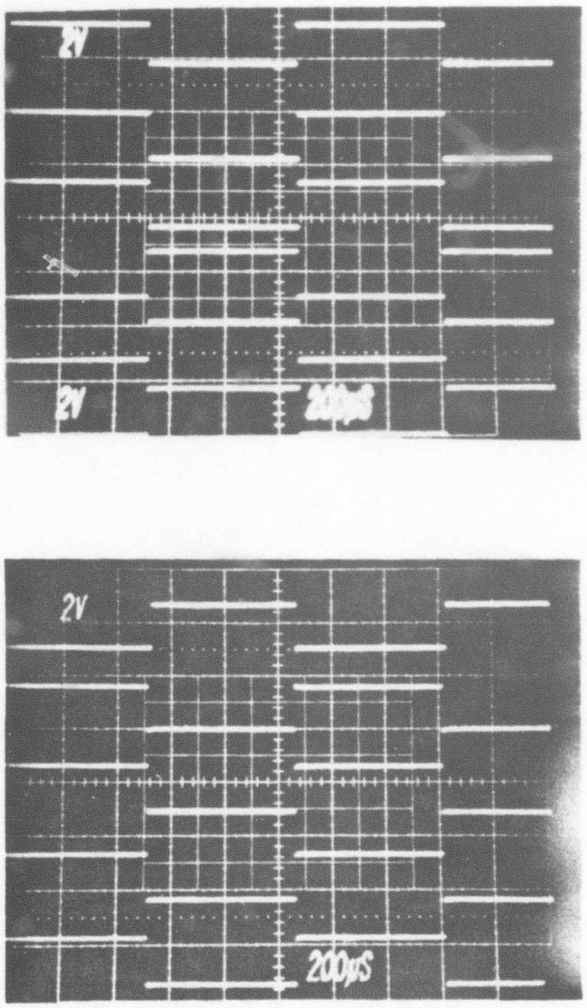



Fig. 5.1-3 Logic diagram of the control circuits for the 5 x 5 bit parallel multiplier on mask set AR4.

ERC 80-8100




| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| A: | | | | 1 | 1 | 1 | 1 | 1 | |
| B: | | | | 1 | 0 | 0 | 0 | S | |
| | | | | S | S | S | S | S | |
| 1 | 1 | 1 | 1 | 1 | | | | | |
| S | $\overline{S}$ | $\overline{S}$ | $\overline{S}$ | $\overline{S}$ | S | S | S | S | |
| $P_9$ | | | | | | | | | $P_0$ |

Fig. 5.1-4 Outputs from the 5 x 5 bit parallel multiplier with inputs A = 1111 and B = 1000S, or S is the square wave shown in uppermost trace.

High speed testing was also attempted using the on-chip feedback mode. The circuit did exhibit full amplitude oscillations as shown in Fig. 5.1-5. However, the speed of the multiplier was much lower than normal.

During the course of the low speed logic functionality testing it was discovered that the AR4 5 x 5 multiplier contained a serious design error which left the pull-down active loads disconnected from $V_{SS}$ on 16 logic gates in the full adder array. It is certain that this error is responsible for the incomplete functionality and low speed observed. On the other hand, the data are very encouraging because they do not reveal any problem related to process yield. The operating deficiencies are directly traceable to the design error.

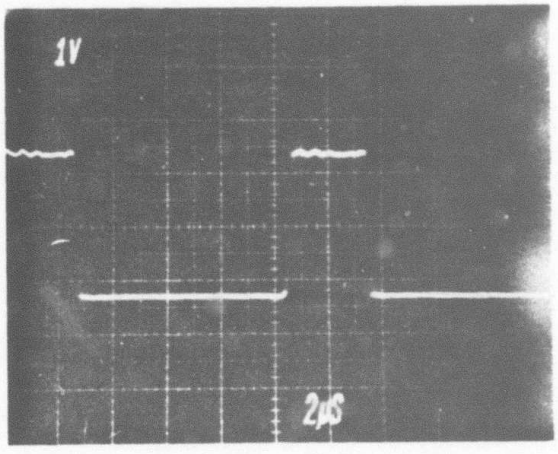
The Schottky metal mask is now being replaced on mask AR4. The design error, has been repaired, and a new mask layer is presently being fabricated. This will allow the following 3 lots of AR4 wafers, which were held before the Schottky metal layer process step, to provide test data on fully working, high speed multiplier circuits.†

## 5.2 2 x 32 Stage Shift Register Evaluation

A photograph of the 2 x 32 stage shift register on the AR4 wafers[2] is shown in Fig. 5.2-1, and a block diagram is shown in Fig. 5.2-2. The circuit consists of 64 D-type flip-flops (D-FF) with a total gate count of 550. The Q output of each stage is connected to the D input of the following stage, so that

†While this report was in press, measurements on the first wafers fabricated after the error correction showed full operation of the 5 x 5 multiplier, at proper speed. The data will be presented in the next report.

ERC 80-8098




$V_{dd}$ = 2.11V $I_{dd}$ = 20.8 mA

$V_{ss}$ = -2.71V $I_{ss}$ = -0.21 mA

$P_D$ = 44.2 mW or 170 μW/GATE

Fig. 5.1-5 Operation of the 5 x 5 bit multiplier in the feedback mode.

ERC80-9097

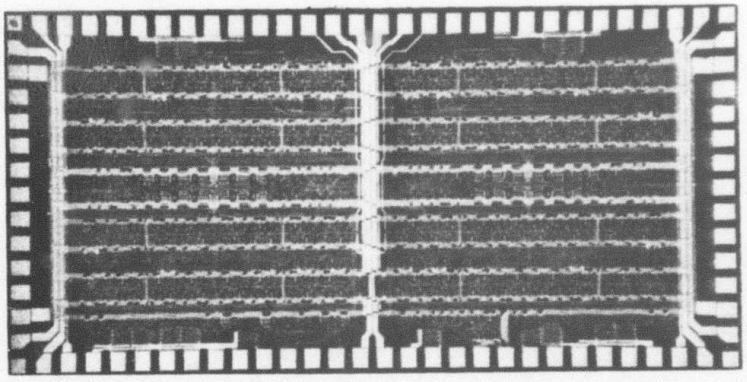


Fig. 5.2-1 Photograph of the 2 x 32-stage shift register fabricated from mask set AR4. This circuit has 550 gates.

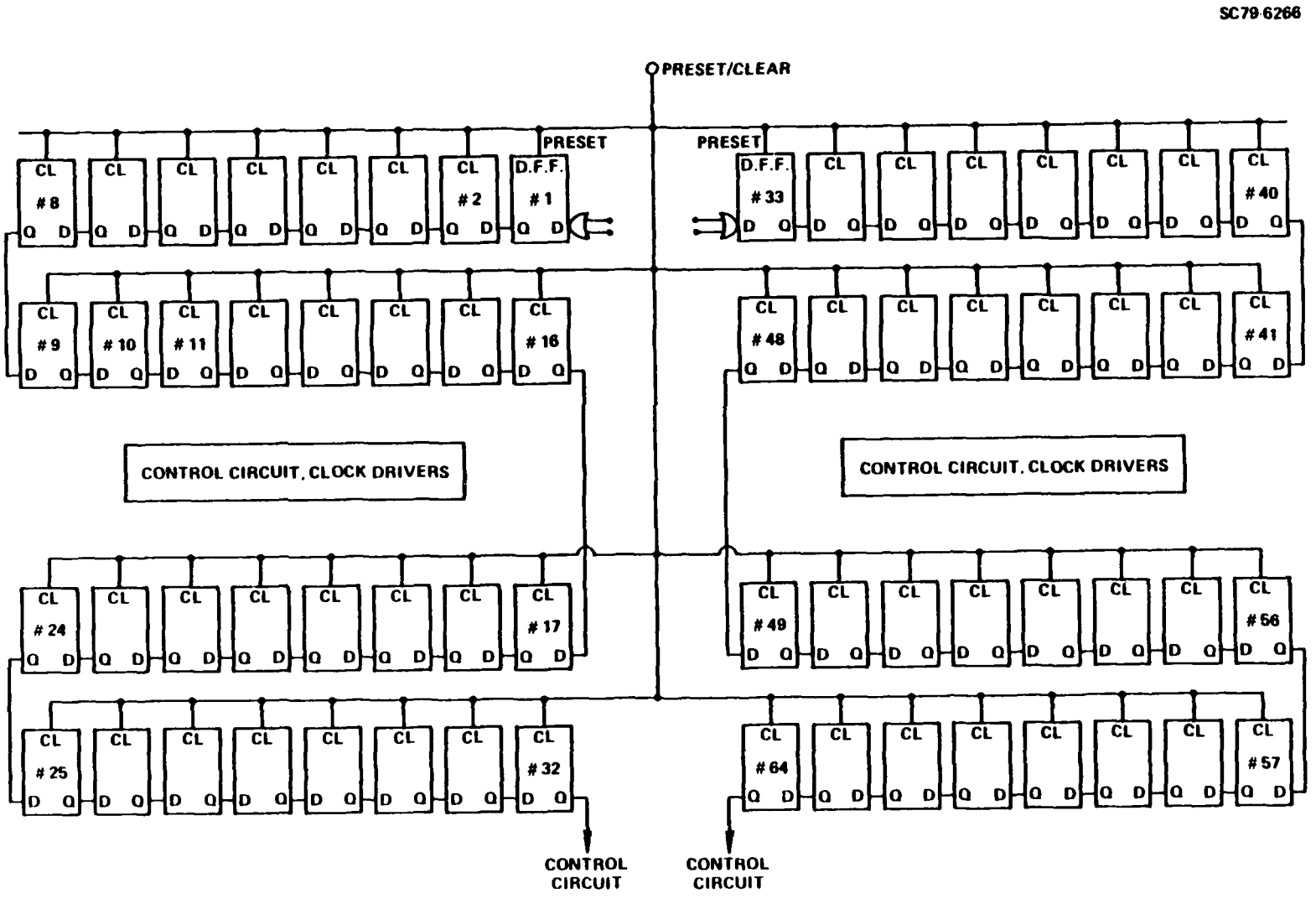



Fig. 5.2-2 Block diagram of the 64-stage shift register on mask set AR4 (from Ref. 2).

data are loaded into the adjacent flip-flop (and thus "shifted") with each trailing edge of the clock pulse. The circuit was described in a previous report.[2]

A control circuit, which consists of 24 NOR gates and three control input lines, is implemented for the control of the operation modes of the 64-stage shift register.[2] A logic diagram of the control circuit is given in Fig. 5.2-3. The five possible operation modes and their required control input conditions are given in the table below the schematic. Control line #1 is designed to enable the serial cascading of the two sets of 32-stage shift registers (to form a 64 stage shift register), control line #2 to disable the operation of P/N generator, and control line #2 activates the serial data in/serial data our operation.

The opertaion of the shift register circuit can be monitored thorugh the buffered output of the 1st, 2nd, 13th, 18th, 28th, 33rd, 34th, 45th, 50th and 60th stages. The evaluation of the shift register circuit has been carried out on the first two AR4 wafer lots fabricated. Partially functional shift registers with more than 33 (out of the 64) registers operational have been found. These devices operated in the serial loading mode where a negative going pulse is fed into the serial data input of the 1st stage D-FF for every 16 clock cycles. The clock driver input to the shift register is shown as the top oscilloscope trace in Fig. 5.2-4. Below the clock trace are shown the inverted output of the 1st stage and the output of the 13th stage delayed by 12 clock pulse with respect to the 1st stage output, as expected. The lowest two traces in Fig. 5.2-4 correspond to the output of the 28th stage and the inverted output

SC79-6341

AR-4 2 x 32 BIT SHIFT REGISTER CONTROL CIRCUIT DIAGRAM

CONTROL #1 ENABLE 1 x 64
CONTROL #2 DIABLE PATTERN GENERATOR
CONTROL #3 ENABLE SERIAL DATA IN

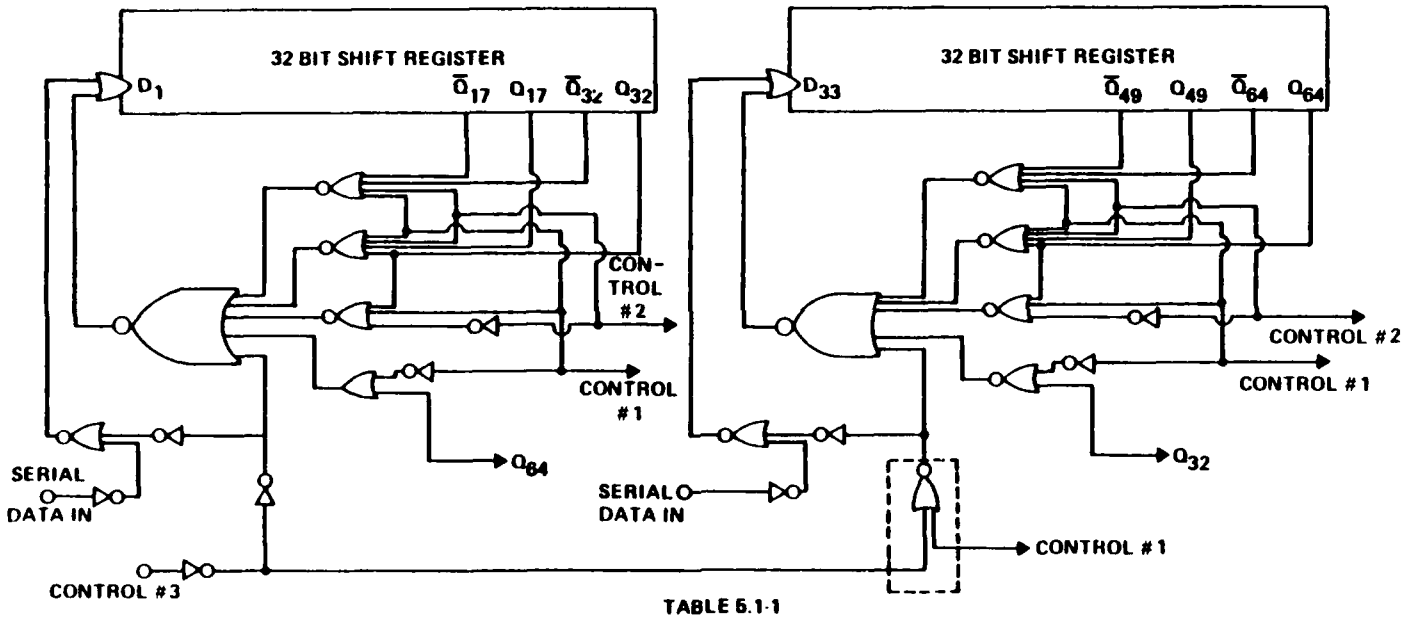



TABLE 6.1-1

| | CONTROL #1 | #2 | #3 | |
|---|---|---|---|---|
| A | 0 | 1 | 0 | 2 x 32 RECIRCULATE |
| B | 0 | X | 1 | 2 x 32 SERIAL DATA IN, SERIAL DATA OUT |
| C | 1 | X | 1 | 1 x 64 SERIAL DATA IN, SERIAL DATA OUT |
| D | 1 | X | 0 | 1 x 64 RECIRCULATE |
| E | 0 | 0 | 0 | 2 x 32 PATTERN GENERATOR |

Fig. 5.2-3 Logic diagram of the control circuit for the 64-stage shift register on mask set AR4 (from Ref. 2).

ERC80-9098

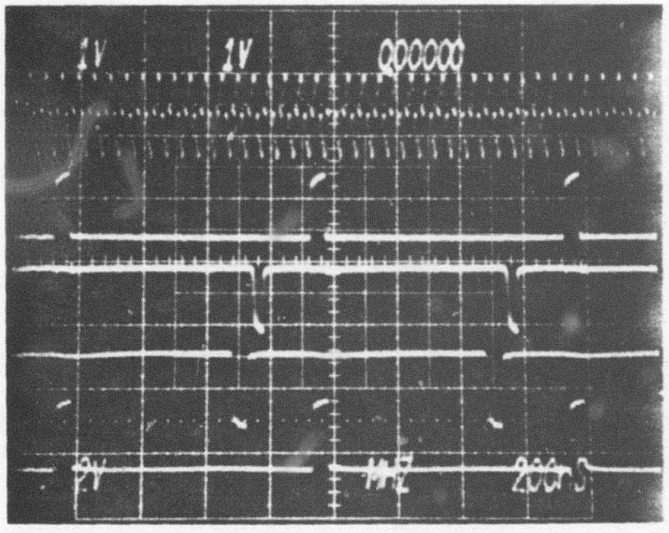



Fig. 5.2-4 2 x 32-stage shift register operating under serial data in 64 stage loop mode.

of the 33rd stage, respectively. These data show that in the 64 bit loop mode, data were properly shifted up to stage 33.

The partial operation of the shift register up to 33 stages indicates that over 300 gates are functioning properly. It is not clear at this point what is the cause for the incomplete operation. Further evaluation will be carried out. Minor design changes were made on the AR4 Schottky metal mask (modified to correct for the design error on the multiplier). These changes may improve the performance on the following wafer lots.

## 5.3 Yield of High Speed Circuits

Statistical data on high speed circuits have not been gathered on a regular basis. The rapid growth of circuit complexity in the current programs makes it difficult to establish systematic statistical measurements. From a yield standpoint, for example, such data become quickly obsolete as circuits become larger. However, an acceptable data base is provided by the results of probing frequency dividers on four wafers tested in order to map potential deliverables.[12] These dividers are no longer on the forefront of the development programs in terms of complexity but they are proven circuits with reasonably high gate counts. The dividers consisted of ÷8 circuits having 25 gates. The ÷8 circuits were on wafers fabricated from mask AR3, having 32 circuits per wafer. The yields are shown in Table 5.3-1.

Table 5.3-1
Yield of Frequency Dividers (÷8, 25 gates)

| Wafer | # Working Devices | Yield |
|---|---|---|
| AR3-69 | 14/32 | 44% |
| AR3-71 | 14/32 | 44% |
| AR3-79 | 11/32 | 34% |
| AR3-81 | 24/32 | 75% |

These are quite satisfactory yields. However, the ÷8 testing was done on the four wafers judged to be the most promising among 16 AR3 wafers available, the main selection criteria being pinchoff voltage values and uniformity of dc device parameters.

The figures reported (up to 75% on 25 gate circuits) are quite satisfactory. At this point the reader must be cautioned against attempting any extrapolation of these yields to larger gate counts based on simple yield equations. Such an extrapolation would lead to very pessimistic conclusions. The reason why such simplistic calculations cannot be made is that the yields reported here are not determined by some fixed "defect" density, but more likely, by our ability to process without flaws, and, perhaps, to the current variations discussed in Section 4.1 of the previous report.[12] Although circuit yields will probably decrease as gate counts increase, the development work is expected to prevent them from falling too rapidly. The success of the program so far basically amounts to having achieved this goal.

## 5.4 Radiation Hardness Assessment

The successful application of GaAs high speed digital circuits in a space environment is dependent upon a sufficiently large total dose radiation hardness. While GaAs MESFET ICs are expected to be superior to silicon MOS devices (small device area, no oxide, semi-insulating substrate), this expecta-

tion confirmed by preliminary results, must be verified by experiments on GaAs planar ICs. A summary of data from total dose radiation hardness evaluation reported for a variety of GaAs devices is presented in Table 5.4-1. It can be seen from this table that GaAs total dose hardness is very promising for ICs, CCDs, JFETs and discrete MESFETs. A total dose of $10^6$ rads is considered to be worst case exposure for typical satellite applications. Degradation mechanisms reported in the literature[13-15] for GaAs devices are threshold voltage shift and mobility degradation. However, for FET channels doped at $10^{17}$ $cm^{-3}$ these effects have been insignificant even at $10^8$ rads doses.

Table 5.4-1
Radiation Hardness (Total Dose)

| Device | Total Dose (rad) (X-ray or Gamma) | Results |
|---|---|---|
| GaAs IC dividers (÷8) (Rockwell) | $5 \times 10^7$ | No change of maximum clock rate |
| GaAs CCD (Rockwell) | $2 \times 10^6$ | No observable gate threshold shifts |
| GaAs Enhancement-Mode JFET Ring Oscillator [13, 14] | $10^7$ | Negligible threshold shift or current degradation |
| GaAs MESFET-Discrete [15] | $8 \times 10^7$ | Negligible threshold shift or current degradation |

Preliminary experiments on Rockwell GaAs planar integrated circuits (first row on Table 5.4-1) are very promising. Three packaged ÷8 circuits[12] were irradiated at RADC with total gamma doses of $10^6$, $10^7$ and $5 \times 10^7$ rad respectively. The circuits were found fully operational after irradiation. The maximum clock rates, of 1.1 GHz for all circuits, had not changed. The only noticeable changes were small variations in the optimum bias voltages and corresponding currents. However, these small changes may be attributed to uncertainties in the test fixture. These excellent results tend to confirm the expectations for GaAs ICs. However, a thorough investigation is needed.

## 6.0 CIRCUIT DESIGN/8 x 8 MULTIPLIER ON MASK SET AR5

Design, layout and digitization of mask set AR5 have been completed. This mask contains in its CD chip one large circuit, an 8 x 8 bit parallel multiplier, occupying almost all the chip area. The dimensions of the multiplier are 2.7 x 2.25 mm. The gate count is 1000 gates (including drivers and test control logic). The PM chip on mask AR5 is a direct copy from AR4 with only minor changes.

The 8 x 8 multiplier forms the 16 bit product of two 8 bit input numbers. The multiplication is done in parallel by an array multiplier similar to the 3 x 3 or 5 x 5 multiplier described in previous reports[2,16] and the input and output words can be latched or the input can be entered directly under external control. Control of the latching, as well as the clocking, is separate for input and output. An externally activated feedback self test connection is included, similar to the one on the 3 x 3 and 5 x 5 multipliers.[2,16] A block diagram is shown in Fig. 6.0-1.

An array multiplier implements the operations involved in multiplication in a straightforward way. The multiplication of two 8 bit numbers A = $a_7a_6...a_j...a$, and B = $b_7b_6..b_k..b_1b_0$ involves the sequential addition of partial sum and product terms which depend, initially, on terms that are the logical AND of individual bits of A and B, and are in the form $a_jb_k$. Fig. 6.0-2 depicts these operations; shown are the required bit combinations, with blocks being used to indicate adders, and arrows to indicate connection of sum and carry adder outputs to subsequent adders. Each adder block is thus adding the $a_jb_k$ term(s) shown inside and the one bit numbers represented by incoming arrows. Note that each adder block adds either two or three terms corresponding to half or full adders. In fact, the arrangement is an array of full adders except for the top row and lower right corner, which are half adders. The appropriate arrangement of adders, showing logic gates and equal interconnections is shown in Fig. 6.0-3. NOR gates are used to combine the inverses of the input bits, in accordance with the relation $\bar{a}_j + \bar{b}_k = a_j\ b_k$. This array of

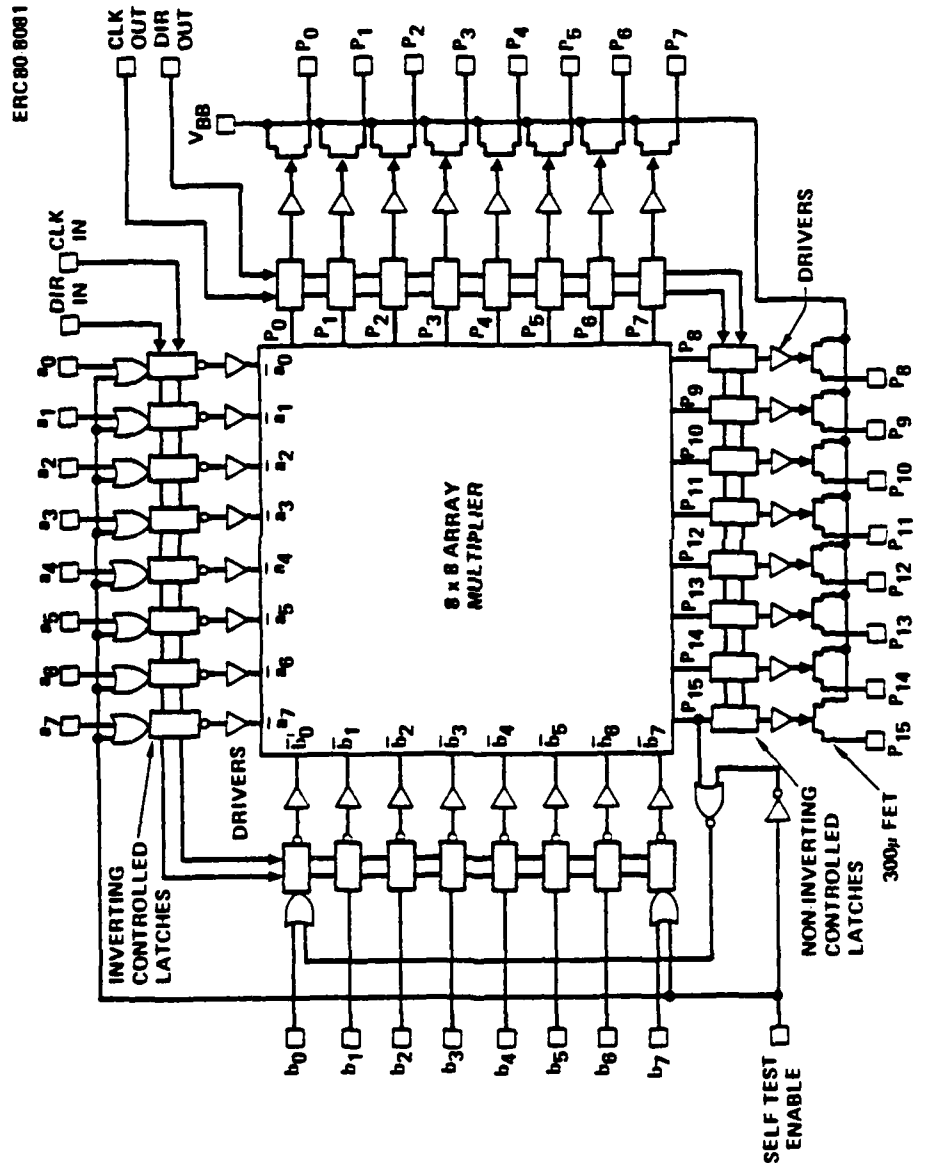



Fig. 6.0-1 Block diagram of the 8 x 8 parallel multiplier. Self test feedback path is shown on this figure.

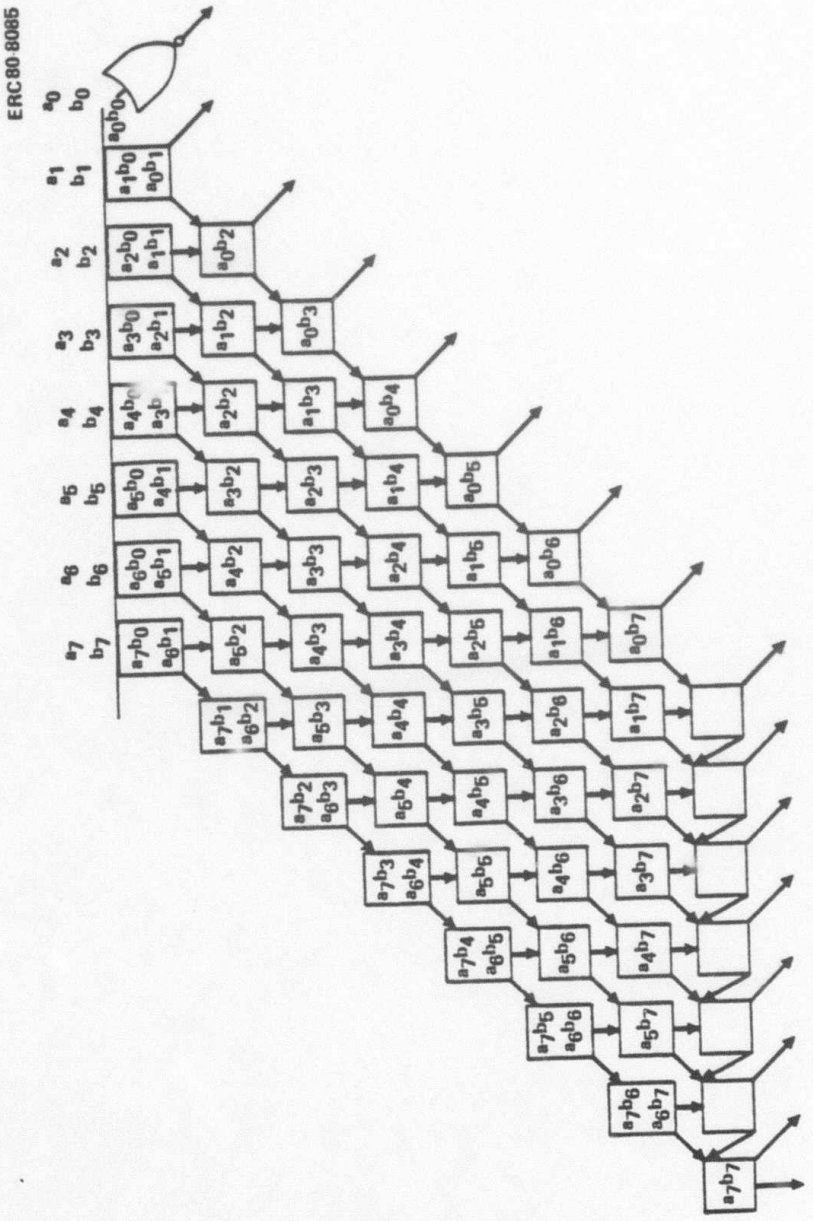



Fig. 6.0-2 Full adder array illustrating the multiplication of two 8-bit numbers.

ERC80-8084

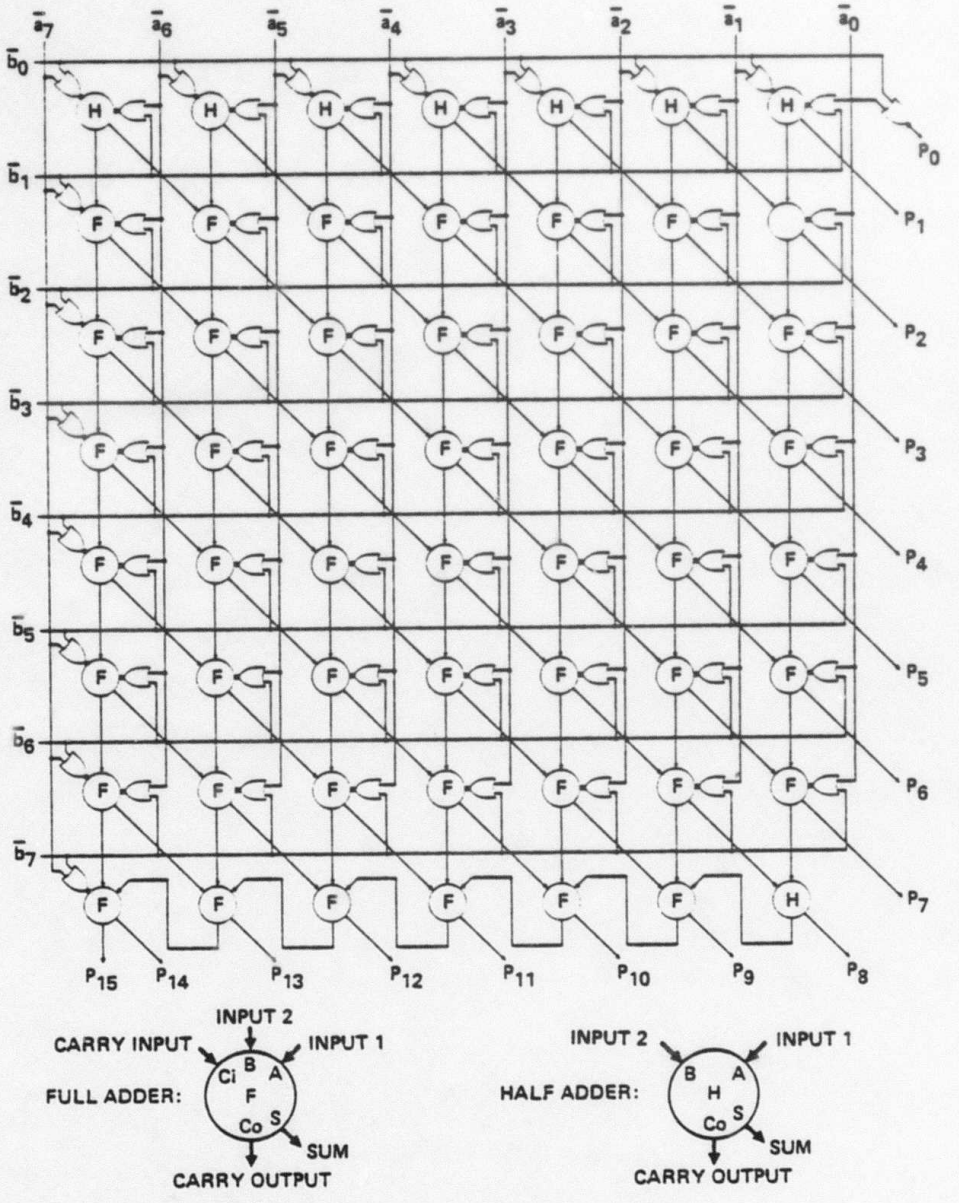



Fig. 6.0-3 Circuit diagram of 8 x 8 parallel multiplier array.

half and full adders and gates forms the 8 x 8 array multiplier part of the circuit.

The outputs of the array go through non-inverting controlled latches, to drivers, and then to output FETs. The non-inverting controlled latch is essentially a D flip-flop with a bypass, as shown in Fig. 6.0-4. When the direct control line is "high," the input is routed to the output through two gates. When the direct control line is low, the input becomes latched under control of the clock, in normal D flip-flop fashion. The inverting controlled latch is just a modification of the non-inverting one.

The inputs enter via inverting controlled latches, and complementary drivers. The drivers are required to drive the considerable capacitance of the array; by implementing them in complementary form, dc power is minimized.

The self-test feedback circuit (see Fig. 5.1-3 for the 5 x 5 multiplier) is activated by holding the enable line high. This applies "ones" to all $a_j$ lines and to $b_7$. It also applies the complement of output bit $P_{15}$ to $b_0$. This connection is unstable, as can be seen from the multiplication:

$$
\begin{array}{r}
A = 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\
B = 1\ 0\ 0\ 0\ 0\ 0\ 0\ b_0 \\
\hline
b_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 \\
1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\
\hline
b_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0
\end{array}
$$

Changing bit $b_0$ (from 1 to 0 or 0 to 1) involves the longest delay path through the multiplier array, as can be seen from Fig. 6.0-2 and 6.0-3. Since the delay to a sum output for an SDFL NOR implemented adder is $3\tau_d$ and for a carry is $2\tau_d$, the delay to the most significant product bit ($P_{15}$) is 6 sums and 8 carries for a total of $34\tau_d$. Adding the control and latch gates, the self test mode causes the multiplier to self oscillate with half-period of $\sim 39\tau_d$.

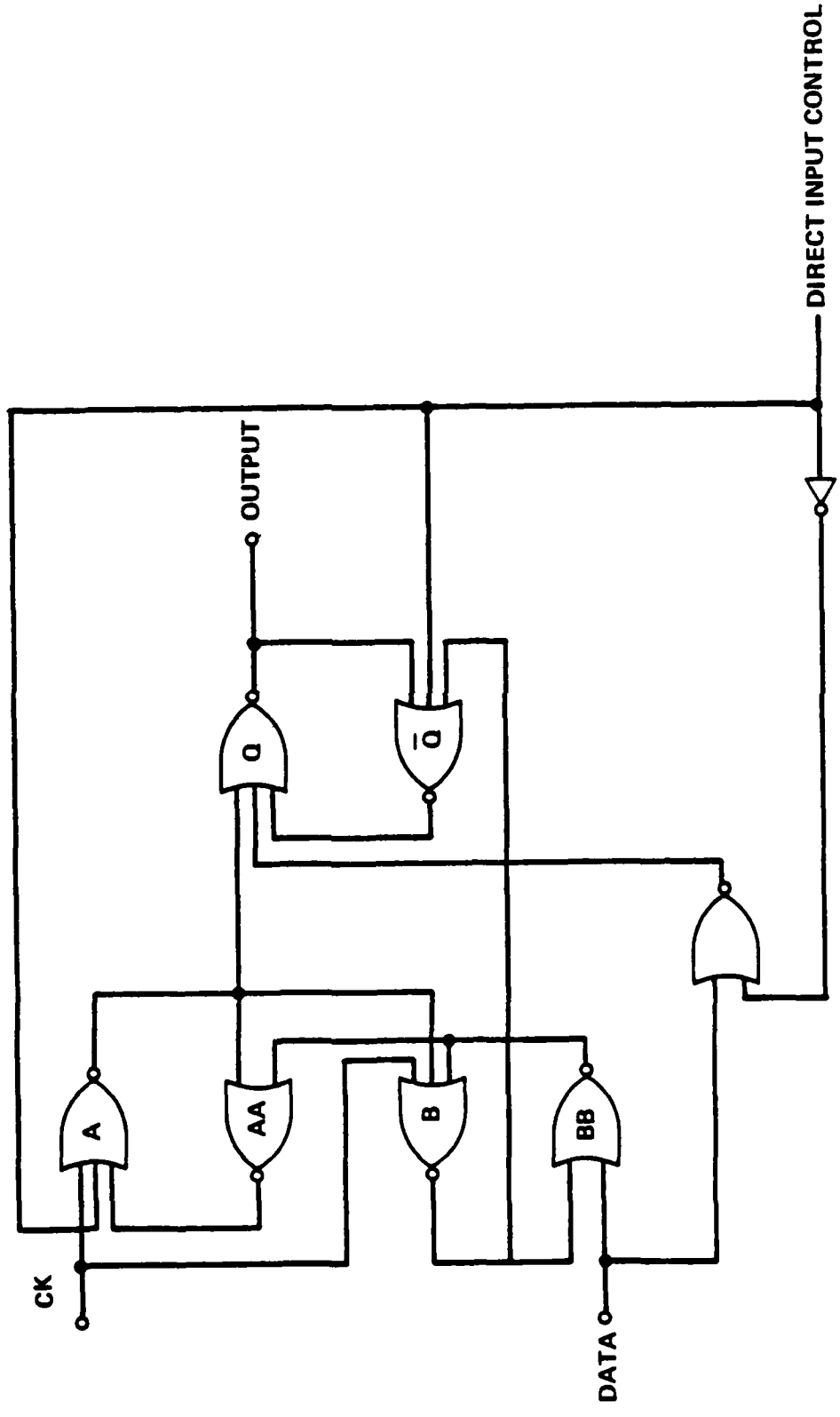



Fig. 6.0-4 Circuit diagram of non-inverting control latch.

Operation is therefore possible in three modes; with inputs and outputs unlatched (straight parallel multiplier); with inputs and/or outputs latched and independently clocked; and in an oscillatory self test mode. The 8 x 8 multiplier clearly represents an LSI chip. The array multiplier has 688 gates and the latches add 256 for 944. Including driver and control gates, the total is 1008.

The layout is designed in a very modular form. The full and half adders are organized as cells, as are the inverting controlled latch (ICL) and the non-inverting controlled latch (NICL). The layout is then as shown in Fig. 6.0-5. The chip size, 2.7 mm by 2.25 mm, results in fairly long bit lines with attendant high capacitance. The complementary switched bit drivers have been designed accordingly, to provide for 100 ps switching of the signals on the lines, in spite of this capacitance.

The worst case delay through the circuit, for input to 16 bit product is approximately $40\tau_d$, including $35\tau_d$ for the array, $3\tau_d$ for the input latch bypass, and $2\tau_d$ for the output latch bypass. A $\tau_d$ of approximately 100 ps would provide a 16 bit product in 4 ns, which is the anticipated speed of operation.

Processing of wafers using mast set AR5 will begin shortly, when fabrication of the masks is completed.

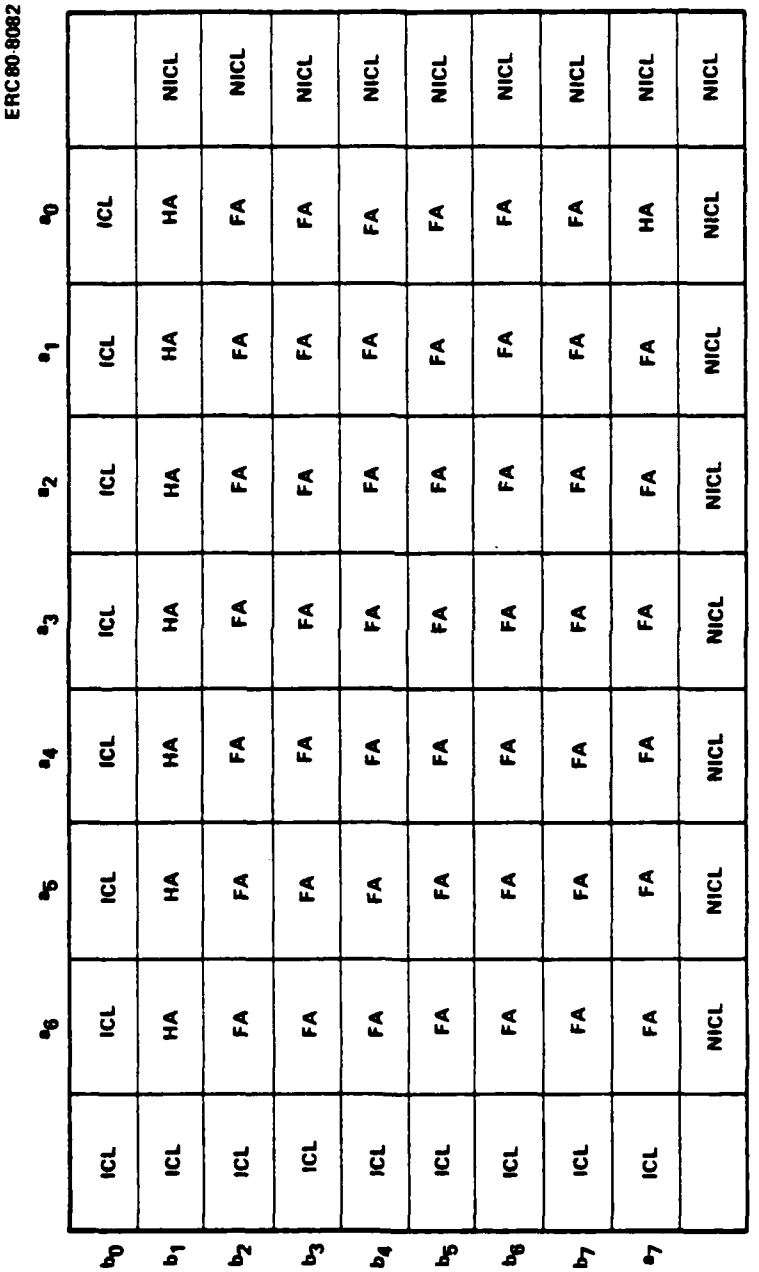



Fig. 6.0-5 Layout of 8 x 8 multiplier. This multiplier is designed of an array of cells consisting of inverting control latches, non-inverting control latches, half adders, and full adders.

## 7.0 REFERENCES

1. R. Zucca et al., "Ion Implanted GaAs IC Process Technology," Quarterly Technical Report No. 8, Contract No. F49620-77-C-0087, August 1979.

2. R. Zucca et al., "Ion Implanted GaAs IC Process Technology," Quarterly Technical Report No. 9, Contract No. F49620-77-C-0087, December 1979.

3. R.D. Fairman and J.R. Oliver, "Growth and Characterization of Semi-Insulating GaAs for Use in Ion Implantation," Proc. Semi-Insulating III-V Materials Conference, Nottingham, April 1980 (in press).

4. T.J. Magee, J. Peng, J.D. Hong, V.R. Deline and C.A. Evans, Jr., Appl. Phys. Lett. 35, 615 (1979).

5. T.J. Magee, J. Hong, V.R. Deline and C.A. Evans, Jr., to be published in Appl. Phys. Lett.

6. F.H. Eisen and B.M. Welch, Proc. 5th Internatinal Conf. on Ion Implantation in Semiconductors and Other Materials, p. 97 (1976).

7. H. Paria and H. Hartnagel, Appl. Phys. 10, 97 (1976).

8. K. Heime, U. König, E. Kohn and A. Wartmann, Solid-State Electron. 17, 835 (1974).

9. K.N. Tu and J.W. Mayer, in Thin Films - Interdiffusion and Reactions, J.M. Poate, K.N. Tu and J.W. Mayer, Eds., (J. Wiley, New York, 1978), p. 359.

10. A.K. Sinha, T.E. Smith and H.J. Levinstein, IEEE Trans. Elect. Dev. ED-22, 218 (1975).

11. H.H. Berger, Solid-State Electron. 15, 145-158 (1972); J. Electrolchem. Soc. 119, 507 (1972).

12. R. Zucca et al., "Ion Implanted GaAs IC Process Technology," Quarterly Technical Report No. 10, Contract No. F49620-77-C-0087, March 1980.

13. R. Zuleeg, J. Notthoff and K. Lehovec, "Enhancement Mode GaAs JFET Medium Scale Integrated Circuit Technology," AFAL-TR-78-25 (1978).

14. R. Zuleeg, J. Notthoff and K. Lehovec, "Radiation Effect in Enhancement Mode GaAs Junction FETs," IEEE Trans. on Nucl. Sci., NS-25, pp. 2305-2308, 1978.

15. J.M. Borrego, R.J. Gutmann, S.B. Moghe and M.J. Chudzicki, "Radiation Effects on GaAs MESFETs," IEEE Trans. on Nucl. Sci., NS-25, pp. 1436-1443, 1978.

16. R. Zucca et al., "Ion Implanted GaAs IC Process Technology," Quarterly Technical Report No. 7, Contract No. F49620-77-C-0087, June 1979.